Linear Charger for 1Cell Li-ion Battery with System-path IC
Monolithic IC MM3538AL

Outline

This IC is a linear charging control IC with built-in system paths, and includes a chip with system path function and lithium ion/lithium polymer secondary battery charging function.
This IC features a built-in load switch with overvoltage detection function and input current limit required for system paths, and built-in power FETs, backflow prevention diodes, and current sensor function required for charging and discharging.
The IC comes equipped with an adapter and USB automatic recognition function, and allows the individual settings for charging control voltage and current with I² C communication.

Features

(1) ADP/USB detection by using of USB bus D+/D- pin
(2) I²Cbus control CC/CV/Charge ON/OFF
(3) Support for JEITA battery temperature profile
(4) System path current limit of ADP mode is adjustable by ILIM pin
(5) 24V High Voltage torelance(IN pin)
(6) Support for operating system out from battery (built-in low on resistance FET)
(7) Linear charger control for Li-ion,Li-pol
(8) Charge current setting by ISET pin
(9) Charge timer setting by TMR pin
(10) Indicator : Input power connected (INGOOD pin)
Charge condition (CHG pin)
BAT voltage condition (OUTGOOD pin)
I²C alarm(SAL pin).

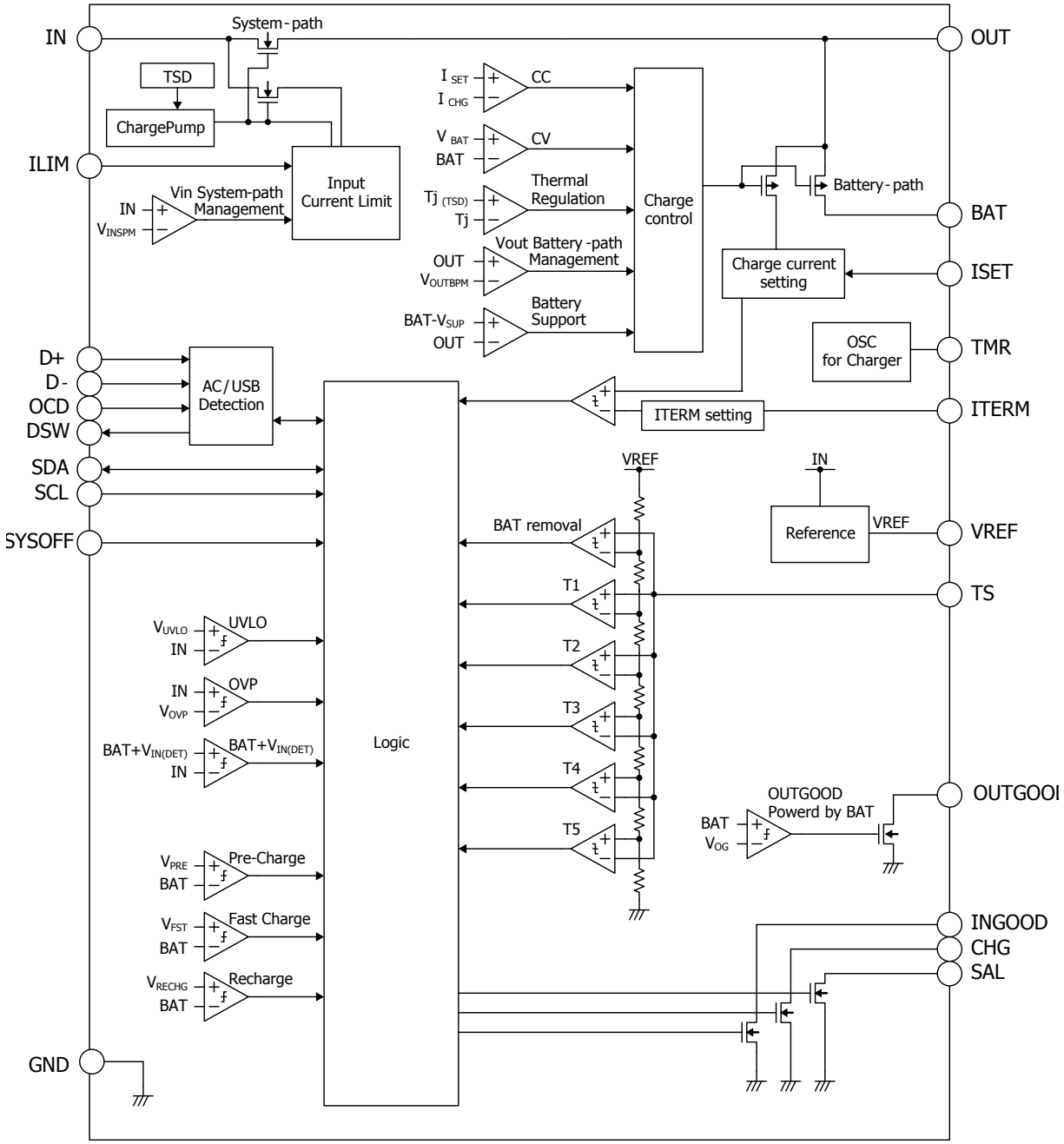
Package

WLCSP-25A

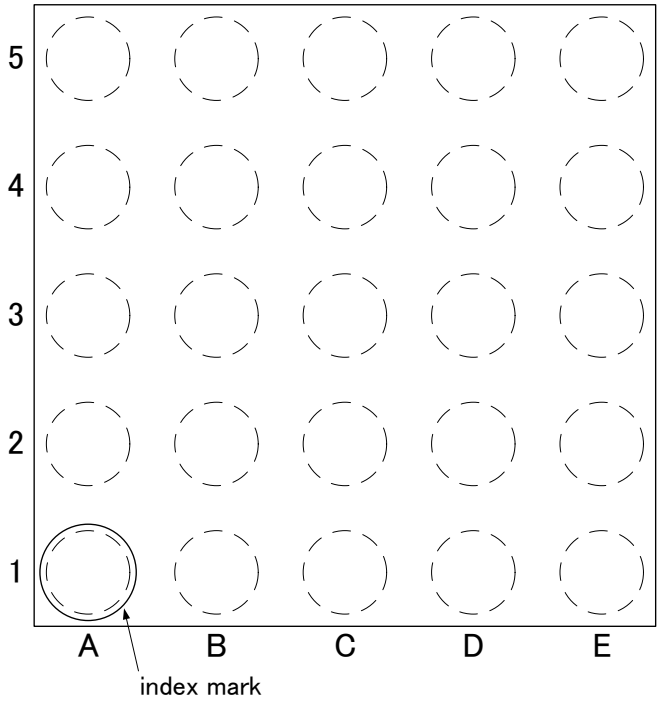
Applications

(1) Tablets
(2) Smartphones
(3) Digital still cameras
(4) Portable music players
(5) Portable games

Block diagram



Pin assinmet



(TOP VIEW)

Pin No.	Function
A1	IN
A2	ILIM
A3	D–
A4	D+
A5	GND
B1	INGOOD
B2	OCD
B3	DSW
B4	SAL
B5	OUTGOOD
C1 C2 D2	OUT
C3	ISET
C4	SDA
C5	TMR
D1 E1 E2	BAT
D3	TS
D4	SCL
D5	CHG
E3	VREF
E4	SYSOFF
E5	ITERM

Pin Description

Pin No.	Symbol	Function
A1	IN	Power supply input pin that connects AC adaptor or USB.
A2	ILIM	System-path current limit setting. Connect a resistor between this pin and GND.
A3	D-	USB bus D- input.
A4	D+	USB bus D+ input.
A5	GND	Ground pin.
B1	INGOOD	Input OK indicator. NchMOS open drain output.
B2	OCD	Default System-path current limit setting when USB detected. Input H/L.
B3	DSW	Control pin for external USB signal switch. Inverter output.
B4	SAL	I^2C alarm indicator. NchMOS open drain output.
B5	OUTGOOD	Output OK indicator. NchMOS open drain output.
C1 C2 D2	OUT	System-path output pin. Output power to the system.
C3	ISET	Charge current setting pin. Connec a resistor between this pin and GND.
C4	SDA	I^2C data input and output pin.
C5	TMR	Oscillator frequency setting pin for the charge timer. Connect a capacitor between this pin and GND.
D1 E1 E2	BAT	Li-ion battery connection pin. Charging to Li-ion battery and discharging to OUT pin.
D3	TS	Thermistor input pin. Connect the terminal of the battery pack thermistor.
D4	SCL	I^2C clock input pin.
D5	CHG	Charge status indicator. NchMOS open drain output.
E3	VREF	Battery thermistor reference voltage output. Connect TS pin through a resistor.
E4	SYSOFF	Turn off System-path. Input H/L.
E5	ITERM	End-of-charge current setting pin. Connect a resistor between this pin and GND.

Absolute Maximum Ratings

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Ratings	Units
Storage temperature	Tstg	–55 ～ +150	℃
Junction temperature	Tj_{MAX}	–40 ～ +150	℃
IN pin input voltage	$VHin_{MAX}$	–0.3 ～ +24	V
Other pin input voltage	Vin_{MAX}	–0.3 ～ +6.0	V
IN pin input current	IIN_{MAX}	～ 2.0	A
OUT pin output current	$IOUT_{MAX}$	～ 5	A
BAT pin input and output current	$IBAT_{MAX}$	～ 5	A
Power dissipation(*1)	Pd	～ 1.0	W

(*1) Board size：80mm × 70mm × 1.6mm Material：grass epoxy Layer：2Layers Wire rate：90%

Recommended Operation Conditions

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Ratings	Units
Operating ambient temperature(*2)	Topr	–40 ～ +85	℃
Junction temperature	Tj	–40 ～ +125	℃
IN pin input voltage	VHin	4.35 ～ 5.5	V
Other pin input voltage	Vin	0 ～ 5.5	V
ILIM setting resistance	R_{ILIM}	40 ～ 400	kΩ
ISET setting resistance	R_{ISET}	53.33 ～ 400	kΩ
ITERM setting resistance	R_{ITERM}	40 ～ 400	kΩ
TMR setting capacitor	C_{TMR}	5 ～ 50	nF

(*2) Board size：80mm × 70mm × 1.6mm Material：grass epoxy Layer：2Layers Wire rate：90%

Electrical Characteristics

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
POWER SUPPLY INPUT						
Consumption current 1	Icc	IN=5V, SYSOFF="L" IN pin input current		1.2	2.0	mA
Consumption current 2	Icc_{OFF}	IN=5V, SYSOFF="H" IN pin input current		300	500	uA
Consumption current 3	Icc_{BAT}	BAT=4.2V, IN=0V BAT pin input current		4	10	uA
Under voltage lock-out	V_{UVLO}	IN=L → H	3.1	3.2	3.3	V
Hysteresis on V_{UVLO}(*3)	V_{UVLO}hys	IN=H → L		100		mV
Overvoltage protection	V_{OVP}	IN=L → H	5.6	5.7	5.8	V
Hysteresis on V_{OVP}(*3)	V_{OVP}hys	IN=H → L		175		mV
Input power detection voltage	$V_{IN(DET)}$	BAT=3.6V, IN=L → H Input power detect when IN ≧ BAT+$V_{IN(DET)}$	50	80	130	mV
Hysteresis on $V_{IN(DET)}$(*3)	$V_{IN(DET)}$hys	BAT=3.6V, IN=H → L	20	35	50	mV
Input power detection deglitch time(*3)	$t_{DGL(IN)}$	Time measured from IN=0 → 5V(1us rise-time) to INGOOD="L"		1.0		ms
Overvoltage blanking time(*3)	$t_{DGL(OVP)}$			50		us
OVP recovery deglitch time(*3)	$t_{DGL(REC)}$	Time measured from IN=10 → 5V(1us fall-time) to INGOOD="L"		1.0		ms
Input power loss to OUT turn-off delay time(*3)	t_{DELAY}	BAT=3.6V Time measured from IN=5 → 3V(1us fall-time) to INGOOD="H"		10		ms
Thermal shutdown temperature(*3)	$Tj_{(TSD)}$	Tj=L → H		150		℃
Hysteresis on $Tj_{(TSD)}$(*3)	$Tj_{(TSD)}$hys	Tj=H → L		30		℃

(*3) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
SYSTEM-PATH・BATTERY-PATH						
Input current limit	I_{LIM1}	OUT=3.6V	80	90	100	mA
	I_{LIM2}	OUT=3.6V	450	475	500	mA
	I_{LIM3}	OUT=3.6V		K_{ILIM} /R_{ILIM}		A
ILIM setting current range(*4)	$I_{LIM(RNG)}$		200		1,500	mA
ILIM setting factor	K_{ILIM}	I_{LIM3}=1A	72,000	80,000	88,000	AΩ
ON resistance of System-path(*4)	$R_{ON(SYS)}$			200	300	mΩ
ON resistance of Battery-path(*4)	$R_{ON(BAT)}$			50	75	mΩ
Voltage of input current limit operation	V_{INSPM}		4.35	4.50	4.63	V
OUT pin short detection voltage	$V_{OUT(SC)}$		0.8	0.95	1.1	V
Battery support voltage(*4)	V_{SUP}	V_{SUP}=OUT-BAT when Battery support mode BAT=3.8V	150		300	mV

(*4) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
CHARGE CONTROL						
Initialize time(*5)	t_{INIT}	1clk=T_{OSC}		2		clk
Fast charge current setting range(*5)	$I_{CHG(RNG)}$	This is applied to “1 of ISET”	200		1,500	mA
Fast charge current	I_{FSTCHG}	This is applied to “1 of ISET”		K_{ISET} /R_{ISET}		A
Fast charge current setting factor	K_{ISET}	R_{ISET}=160k I_{CHG} ≧ 200mA	76,000	80,000	84,000	AΩ
Fast charge current accuracy @small current	I_{ACC}	R_{ISET}=160kΩ I_{CHG} ＜ 200mA	−10		+10	mA
Pre-charge current	I_{PRECHG}			K_{PRECHG} /R_{ISET}		A
Pre-charge current setting factor	K_{PRECHG}	R_{ISET}=160kΩ	6,000	8,000	10,000	AΩ
Relief charge current	I_{RELCHG}		4	8.5	13	mA
End-of-charge current setting range(*5)	$I_{TERM(RNG)}$	USB 500mA or ILIM mode	20		200	mA
		USB 100mA mode	6.7		66.7	mA
End-of-charge detection current	I_{TERM}			K_{ITERM} /R_{ITERM}		A
End-of-charge detection current setting factor	K_{ITERM}	USB 500mA or ILIM mode R_{ITERM}=160kΩ	6,000	8,000	10,000	AΩ
		USB 100mA mode R_{ITERM}=160kΩ	2,000	2,667	3,333	AΩ
End-of-charge detection deglitch time(*5)	$t_{DGL(TERM)}$	1clk=T_{OSC}		8		clk
BAT pull current(*5)	I_{PULL}			80		mA
BAT pull time(*5)	$t_{BAT(DET)}$			32		ms

(*5) Guaranteed by design

(Except where noted otherwise: Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
Start voltage of pre-charge	V_{PRE}	BAT=L → H	1.9	2.0	2.1	V
Hysteresis on V_{PRE}(*6)	$V_{PRE}hys$	BAT=H → L		100		mV
Start voltage of fast-charge	V_{FST}	BAT=L → H	2.7	2.8	2.9	V
Hysteresis on V_{FST}(*6)	$V_{FST}hys$	BAT=H → L		100		mV
Pre-charge to fast charge transition deglitch time(*6)	t_{PTOF}	1clk=T_{OSC}		16		clk
Constant voltage control (V_{BAT1}>V_{BAT2}>V_{BAT3}>V_{BAT4})	V_{BAT1}		4.17	4.20	4.23	V
	V_{BAT2}		4.12	4.15	4.18	V
	V_{BAT3}		4.07	4.10	4.13	V
	V_{BAT4}		4.02	4.05	4.08	V
Voltage of recharge detection	V_{RECHG}			V_{BAT} -0.20V		V
Voltage of charge current limit operation	V_{OUTBPM}		4.15	4.20	4.25	V
Thermal regulation temperature(*6)	$Tj_{(REG)}$		85	100	115	℃

(*6) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
BATTERY TEMPERATURE DETECTION						
VREF pin output voltage	V_{REF}		2.74	2.80	2.86	V
VREF pin source current ability	I_{REF}	Decrease to 98% of V_{REF}	2			mA
VREF pin leakage current	$I_{VREF(LEAK)}$	V_{REF}=3.1V			1	uA
Battery removal detection TS pin voltage	V_{TBR}	TS=L → H	85.0	90.0	95.0	%V_{REF}
Battery temperature detection TS pin voltage when I²C 05h b07= "0"	V_{T10}	T1 detection TS=L → H	76.6	78.1	79.6	%V_{REF}
	V_{T20}	T2 detection TS=L → H	66.2	67.7	69.2	%V_{REF}
	V_{T30}	T3 detection TS=H → L	27.5	29.0	30.5	%V_{REF}
	V_{T40}	T4 detection TS=H → L	23.4	24.9	26.4	%V_{REF}
	V_{T50}	T5 detection TS=H → L	16.7	18.2	19.7	%V_{REF}
Battery temperature detection TS pin voltage when I²C 05h b07= "1"	V_{T11}	T1 detection TS=L → H	71.6	73.1	74.6	%V_{REF}
	V_{T21}	T2 detection TS=L → H	62.7	64.2	65.7	%V_{REF}
	V_{T31}	T3 detection TS=H → L	31.5	33.0	34.5	%V_{REF}
	V_{T41}	T4 detection TS=H → L	27.9	29.4	30.9	%V_{REF}
	V_{T51}	T5 detection TS=H → L	21.7	23.2	24.7	%V_{REF}
Hysteresis on TS pin voltage detection(*7)	V_{TS}hys			2		%V_{REF}
TS pin leakage current	$I_{TS(LEAK)}$	TS=3.1V			1	uA

(*7) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
OSCILLATOR						
Oscillation period	T_{OSC}	R_{ISET}=160kΩ C_{TMR}=15nF	4.2	6.0	7.8	ms
Pre-charge timer(*8)	T_{PRE}	$T_{BASE}=T_{OSC}\times2^{20}$ I²C default		T_{BASE}		s
Total charge timer(*8)	T_{TOTAL}	$T_{BASE}=T_{OSC}\times2^{20}$ I²C default		6 $\times T_{BASE}$		s
USB DETECTION						
D+/D− detection time(*8)	t_{DDE}			128		ms
D+/D− detection-sw release time(*8)	t_{DRE}			256		ms
Dead time of D+/D−detection(*8)	t_{DSW}			1		ms
DSW pin sink current ability	$V_{DSW(SI)}$	I_{SINK}=1mA when DSW="L"			0.25	V
DSW pin source current ability(*8)	$V_{DSW(SO)}$	I_{SOURCE}=1mA when DSW="H"	4.50			V
Bias at D+ pin(*8)	V_{D+}	can source at least 150uA	0.475	0.600	0.700	V
D+ pin output current limit(*8)	I_{D+}	D+=0V			1.5	mA
D−pin sink current(*8)	I_{D-}	D−=0.5V	10	30	50	uA
D+ pin leakage current	$I_{D+(LEAK)}$	not in detection mode			1	uA
D−pin leakage current	$I_{D-(LEAK)}$	not in detection mode			1	uA
D+/D− comparator threshold	V_{DC}	L → H	0.35	0.40	0.45	V
D+/D−Hysterisis on V_{DC}(*8)	V_{DC}hys	H → L		42		mV

(*8) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

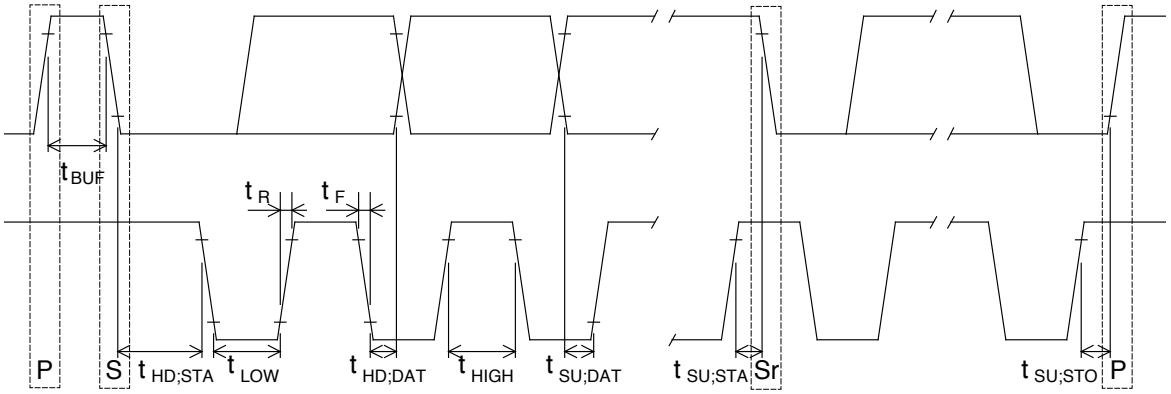
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
OUTGOOD PIN						
OUTGOOD threshold	V_{OG}	BAT=L → H	2.89	2.95	3.01	V
Hysterisis on V_{OG}(*9)	V_{OG}hys	BAT=H → L		0.15		V
LOGIC INPUT AND OUTPUT						
Low level input voltage	V_L	SYSOFF, OCD, SDA, SCL			0.4	V
High level input voltage	V_H	SYSOFF, OCD, SDA, SCL	1.5			V
Built-in pull-down resistor value	R_{PD}	SYSOFF, OCD		100		kΩ
Open drain pin sink current ability	V_{OPD}	I_{SINK}=5mA when Pin="L"			0.25	V

(*9) Guaranteed by design

(Except where noted otherwise : Ta=25℃ , IN=5V)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
I²C BUS						
Clock frequency	f_{SCL}		10		400	kHz
Data transfer wait time(*10)	t_{BUF}		1.3			us
SCL start hold time(*10)	$t_{HD;STA}$		0.6			us
SCL low level hold time(*10)	t_{LOW}		1.3			us
SCL high level hold time(*10)	t_{HIGH}		0.6			us
Start condition setup(*10)	$t_{SU;STA}$		0.6			us
SDA data hold time(*10)	$t_{HD;DAT}$		100			ns
SDA data setup time(*10)	$t_{SU;DAT}$		100			ns
SDA,SCL rise time(*10)	t_R				300	ns
SDA,SCL fall time(*10)	t_F				300	ns
Stop condition setup time(*10)	$t_{SU;STO}$		0.6			us

(*10) Guaranteed by design



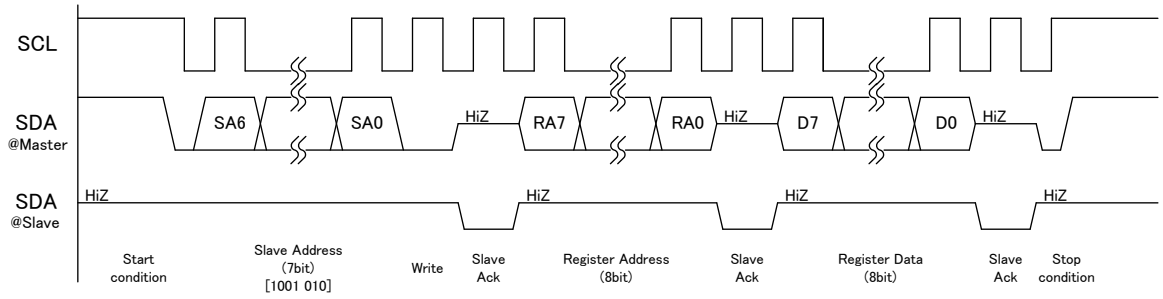
Function

(1) ABOUT I²C BUS

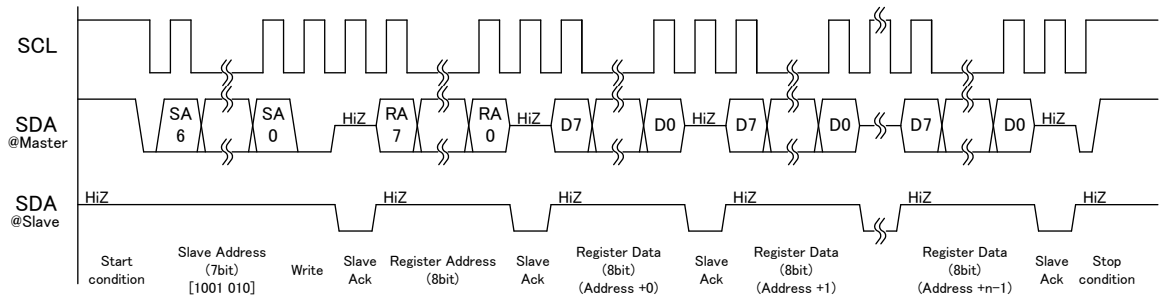
I²C BUS is inter bus system controlled by 2 lines (SDA,SCL). Data are transmitted and received in the units of byte and Acknowledge. It is transmitted by MSB first from the Start condition.

The data format is set as shown in the following figure.

1byte Data Write



n bytes Data Write



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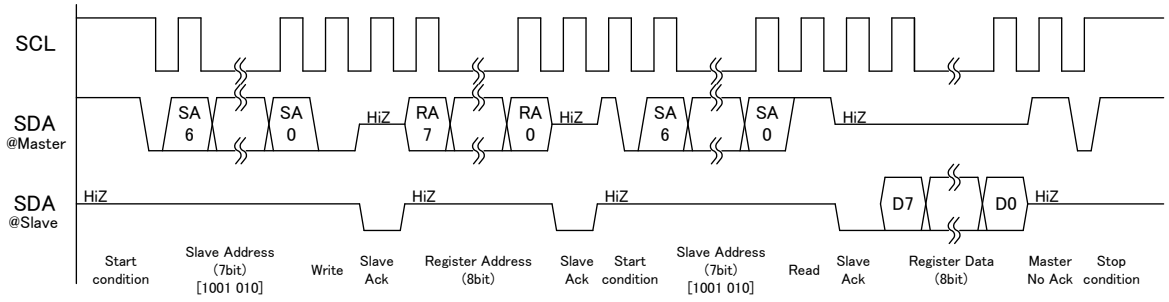
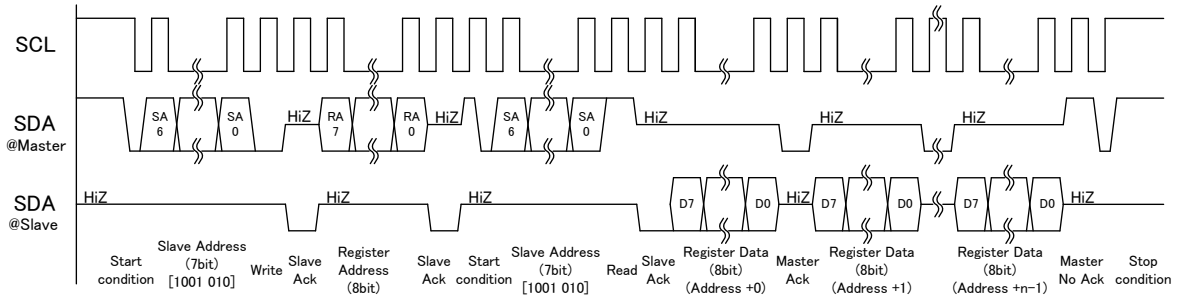


n bytes Data Read



(2) I²C REGISTER MAP

		b07	b06	b05	b04	b03	b02	b01	b00
Slave Address		1	0	0	1	0	1	0	R = 1 W = 0
Register Address	01h	CV Setting (T1 ~ T2)		CV Setting (T2 ~ T3)		CV Setting (T3 ~ T4)		CV Setting (T4 ~ T5)	
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	02h	CC Setting (T1 ~ T2)			CC Setting (T2 ~ T3)			Charge Enable	SAL Release
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	W
	03h	CC Setting (T3 ~ T4)			CC Setting (T4 ~ T5)			USB Current Limit	
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	04h	Battery Temperature			Charger Time-out	Input OVP	ILIM Short	ISET Short	ADP/USB
		R	R	R	R	R	R	R	R
	05h	NTC	Pre-charge Timer			Total charge Timer			
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

R : Read Only (Write data is ignored)
W : Writable ("0" is returned for read-in)
R/W : Readable and Writable

(3) I²C REGISTER EXPLANATION

R/W	CV Setting (T1 ~ T2)		
01h	b07	b06	V
default	0	0	4.05
	0	1	4.10
	1	0	4.15
	1	1	4.20

R/W	CV Setting (T2 ~ T3)		
01h	b05	b04	V
default	0	0	4.05
	0	1	4.10
	1	0	4.15
	1	1	4.20

R/W	CV Setting (T3 ~ T4)		
01h	b03	b02	V
default	0	0	4.05
	0	1	4.10
	1	0	4.15
	1	1	4.20

R/W	CV Setting (T4 ~ T5)		
01h	b01	b00	V
default	0	0	4.05
	0	1	4.10
	1	0	4.15
	1	1	4.20

R/W	CC Setting (T1 ~ T2)			
02h	b07	b06	b05	of ISET
default	0	0	0	1/8
	0	0	1	2/8
	0	1	0	3/8
	0	1	1	4/8
	1	0	0	5/8
	1	0	1	6/8
	1	1	0	7/8
	1	1	1	1

R/W	CC Setting (T2 ~ T3)			
02h	b04	b03	b02	of ISET
default	0	0	0	1/8
	0	0	1	2/8
	0	1	0	3/8
	0	1	1	4/8
	1	0	0	5/8
	1	0	1	6/8
	1	1	0	7/8
	1	1	1	1

R/W	CC Setting (T3 ~ T4)			
03h	b07	b06	b05	of ISET
default	0	0	0	1/8
	0	0	1	2/8
	0	1	0	3/8
	0	1	1	4/8
	1	0	0	5/8
	1	0	1	6/8
	1	1	0	7/8
	1	1	1	1

R/W	CC Setting (T4 ~ T5)			
03h	b04	b03	b02	of ISET
default	0	0	0	1/8
	0	0	1	2/8
	0	1	0	3/8
	0	1	1	4/8
	1	0	0	5/8
	1	0	1	6/8
	1	1	0	7/8
	1	1	1	1

R/W	Charge Enable	
02h	b01	Status
default	0	No charge
	1	Charging

R/W	SAL Release	
02h	b00	Status
default	0	Normal
	1	Release

R/W	USB Current Limit		
03h	b01	b00	Maximum input current
default	0	0	100mA. USB 100mA mode
	0	1	500mA. USB 500mA mode
	1	0	ILIM Setting
	1	1	Standby(USB suspend mode)

R	Battery Temperature			
04h	b07	b06	b05	Status
	0	0	0	Battery not connected
	0	0	1	~ T1
	0	1	0	T1 ~ T2
	0	1	1	T2 ~ T3
	1	0	0	T3 ~ T4
	1	0	1	T4 ~ T5
	1	1	0	T5 ~

R	Charger Time-out	
04h	b04	Status
	0	Normal
	1	Time-out

R	Input OVP	
04h	b03	Status
	0	Normal
	1	OVP

R	ILIM Short	
04h	b02	Status
	0	Normal
	1	Short

R	ISET Short	
04h	b01	Status
	0	Normal
	1	Short

R	ADP/USB	
04h	b00	Status
	0	USB Power
	1	ADP Power

R/W	NTC	
05h	b07	Status
	0	for NCP15WF104F03RC
default	1	for NCP15XH103F03RC

R/W	Pre-charge Timer			
05h	b06	b05	b04	of T_{BASE}
default	0	0	0	1
	0	0	1	2
	0	1	0	3
	0	1	1	4
	1	0	0	5
	1	0	1	6
	1	1	0	7
	1	1	1	No timer

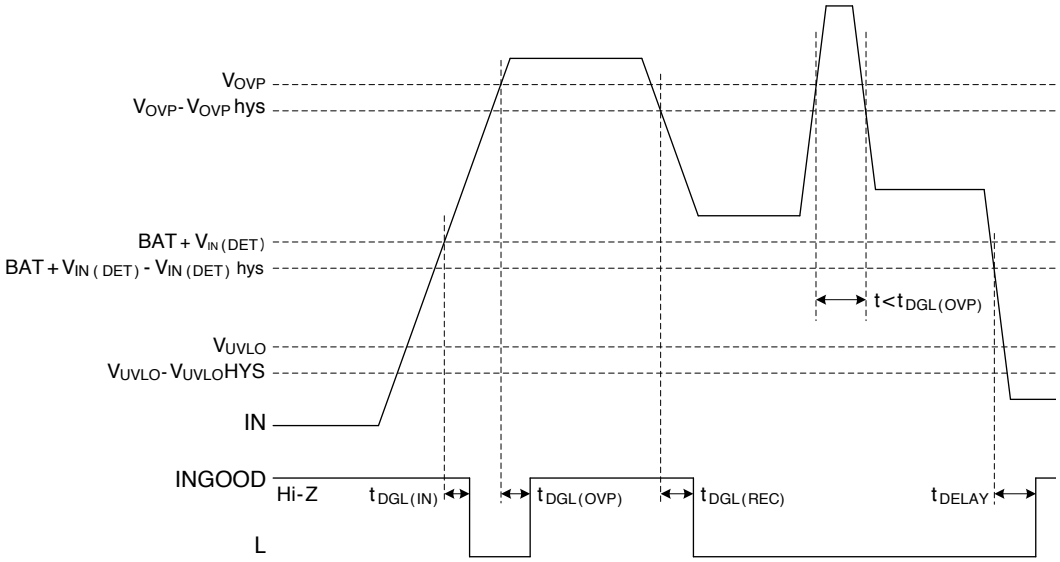
R/W	Total Charge Timer			
05h	b03	b02	b01	of T_{BASE}
	0	0	0	2
	0	0	1	3
	0	1	0	4
	0	1	1	5
default	1	0	0	6
	1	0	1	7
	1	1	0	8
	1	1	1	No timer

(4) POWER SUPPLY INPUT

MM3538 normal operation starts when all the following conditions are met, and determined that the normal power supply is connected.

① IN ＞ VUVLO
② IN ＞ BAT + VIN(DET)
③ IN ＜ VOVP

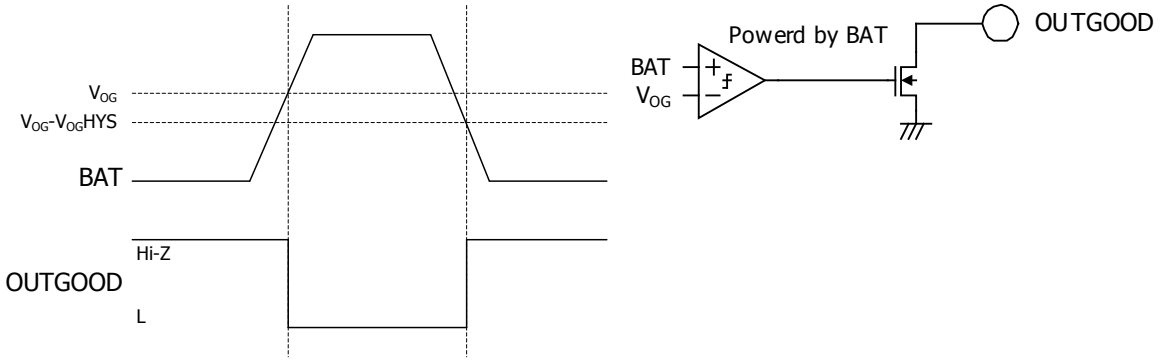
INGOOD pin is NchMOS open drain output. Open drain MOS is turned on when the normal powersupply is connected.



When power is not entered, MM3538 has been on the path to the battery to supply power from the battery to OUT pin.

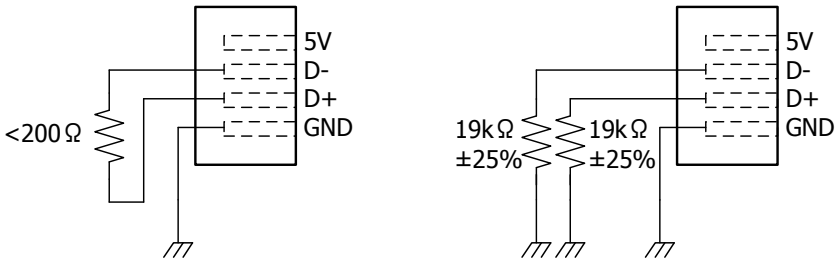
(5) OUTGOOD PIN

OUTGOOD pin is NchMOS open drain output. When BAT pin voltage becomes higher than 2.95V (=VOG), open drain MOS is turned on. Moreover, this function operates on the voltage from BAT pin. For the reason, it operates by battery only.



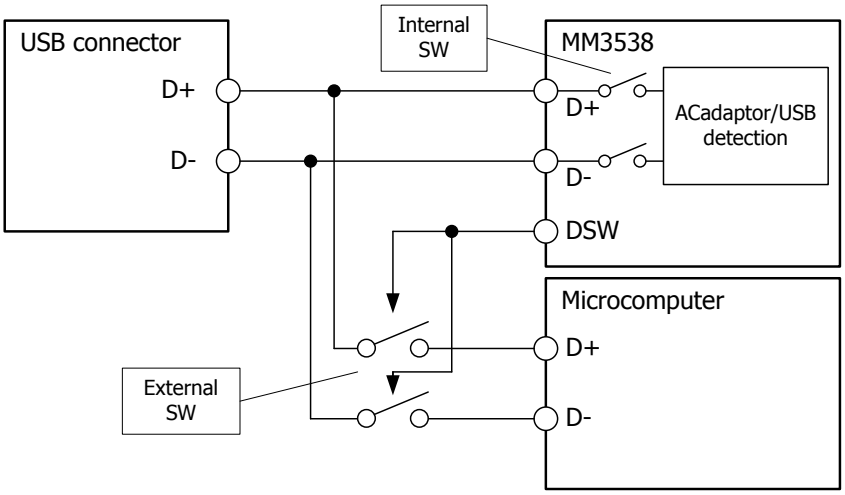
(6) AC ADAPTOR・USB DETECTION

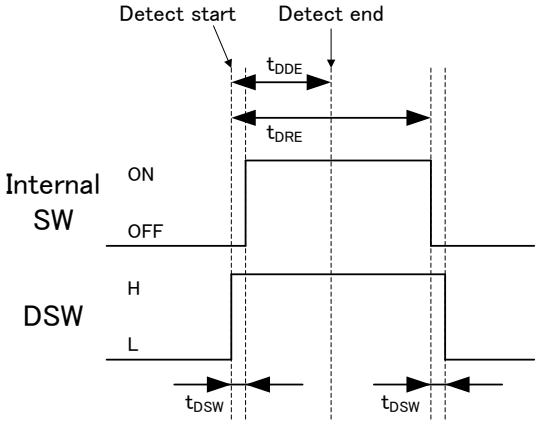
An AC adaptor and USB bus have composition as shown in each following figure. MM3538 uses D+ pin / D− pin, judges automatically whether the inputted power supply is an AC adaptor or a USB bus, and operates an input limit. Moreover, a judgment result is displayed on an I²C register (= I²C 04h b00).



(a) AC adaptor (b) USB

The internal SW is turned on after a power supply input, and detection is started, and detection is ended in 128ms (= tDDE) after. Furthermore, the inside SW is turned off in 128 ms after (a total of 256 ms (=tDRE)). When the inside SW is ON, a DSW terminal outputs "H". As shown in the following figure, it is used for ON/OFF control of the external SW. MM3538 and other ICs will not be simultaneously connected to a D+/D-line.





(7) IN CURRENT LIMIT

MM3538 restricts the system-path current which flows into IN pin.
When detected as USB, the input current limit is set by OCD pin. Then, it can change into other preset values using I²C control. Please refer to another section for OCD pin.
When detected as AC adaptor, the input current limit is set by ILIM pin. Then it can't change into other preset values using I²C control.
The setting current by ILIM pin is as follows.

$$I_{LIM3}\ [A] = \frac{K_{ILIM3}\ [A \cdot \Omega]}{R_{ILIM}\ [\Omega]} = \frac{80{,}000\ [A \cdot \Omega]}{R_{ILIM}\ [\Omega]}$$

(8) OCD PIN

When detected as USB by the AC adaptor/USB detection, it is a terminal which sets up the initial value of an input current limit.
- When OCD="L", input current limit is set to 100mA.
- When OCD="H", input current limit is set to 500mA.

Although an initial value is set up with the above-mentioned value, it can be changed into other preset values after that using I2C control. OCD pin is a terminal which sets up an initial value, after power activation, cannot change a preset value by OCD pin.

(9) IN pin voltage control System-path management (IN-SPM)

MM3538 will decrease an input limit, if IN terminal voltage turns into voltage lower than 4.5V (=VINSPM). Moreover, charge operation is stopped. This function becomes effective only when an input power source is detected as USB, and it prevents crash of USB bus of the host side.

(10) SYSOFF PIN

It is possible to turn off a system-path compulsorily by making SYSOFF pin into "H".

(11) CHARGE CONTROL

Charge is started by making ChargeEnable (=I^2C 02h b01) into "Charging" in the state where there are an input power source and a Li-ion battery. Pre-charge current and Fast charge current will be set up using an ISET pin, and Pre-charge current will be 1/10 of Fast charge current. End-of-charge detection current is set up using ITERM pin. When an input limit is in 100mA mode, End-of-charge detection current is set to one third of the preset values in an ITERM pin. The setting current in ISET pin and ITERM pin is as follows.

$$I_{FSTCHG}[A] = \frac{K_{ISET}[A \cdot \Omega]}{R_{ISET}[\Omega]} = \frac{80{,}000\ [A \cdot \Omega]}{R_{ISET}[\Omega]}$$

$$I_{PRECHG}[A] = \frac{I_{FSTCHG}[A]}{10} = \frac{K_{ISET}[A \cdot \Omega]}{10 \cdot R_{ISET}[\Omega]} = \frac{8{,}000\ [A \cdot \Omega]}{R_{ISET}[\Omega]}$$

$$I_{TERM}[A] = \frac{K_{ITERM}[A \cdot \Omega]}{R_{ITERM}[\Omega]} = \frac{8{,}000\ [A \cdot \Omega]}{R_{ITERM}[\Omega]}$$

Charging current is controlled by general CCCV control. However, charging current decreases during CC control at the following factor developmental time.

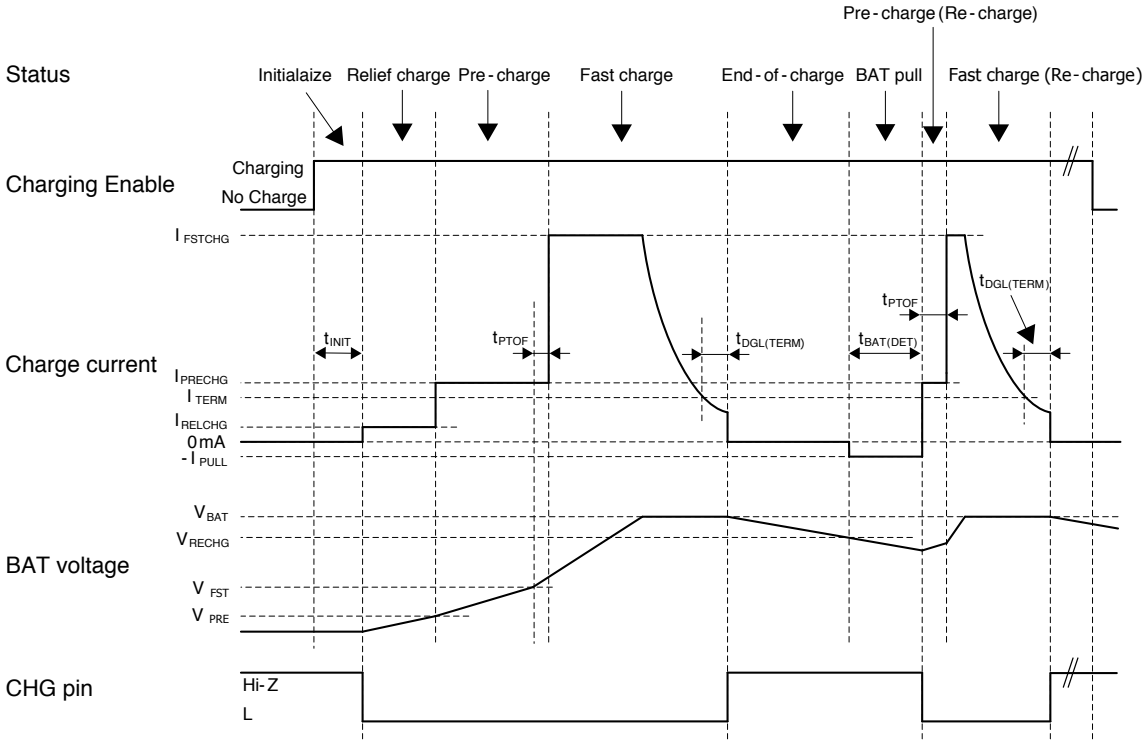
When OUT terminal voltage falls and the charging current limit function operates.
When chip temperature rises and the thermal regulation function operates.

Charge is suspended when the abnormalities in battery temperature occur. And a charger timer stops. A charge timer stops at this time. When these factors are canceled, charge operation is resumed and a charge timer resumes too.

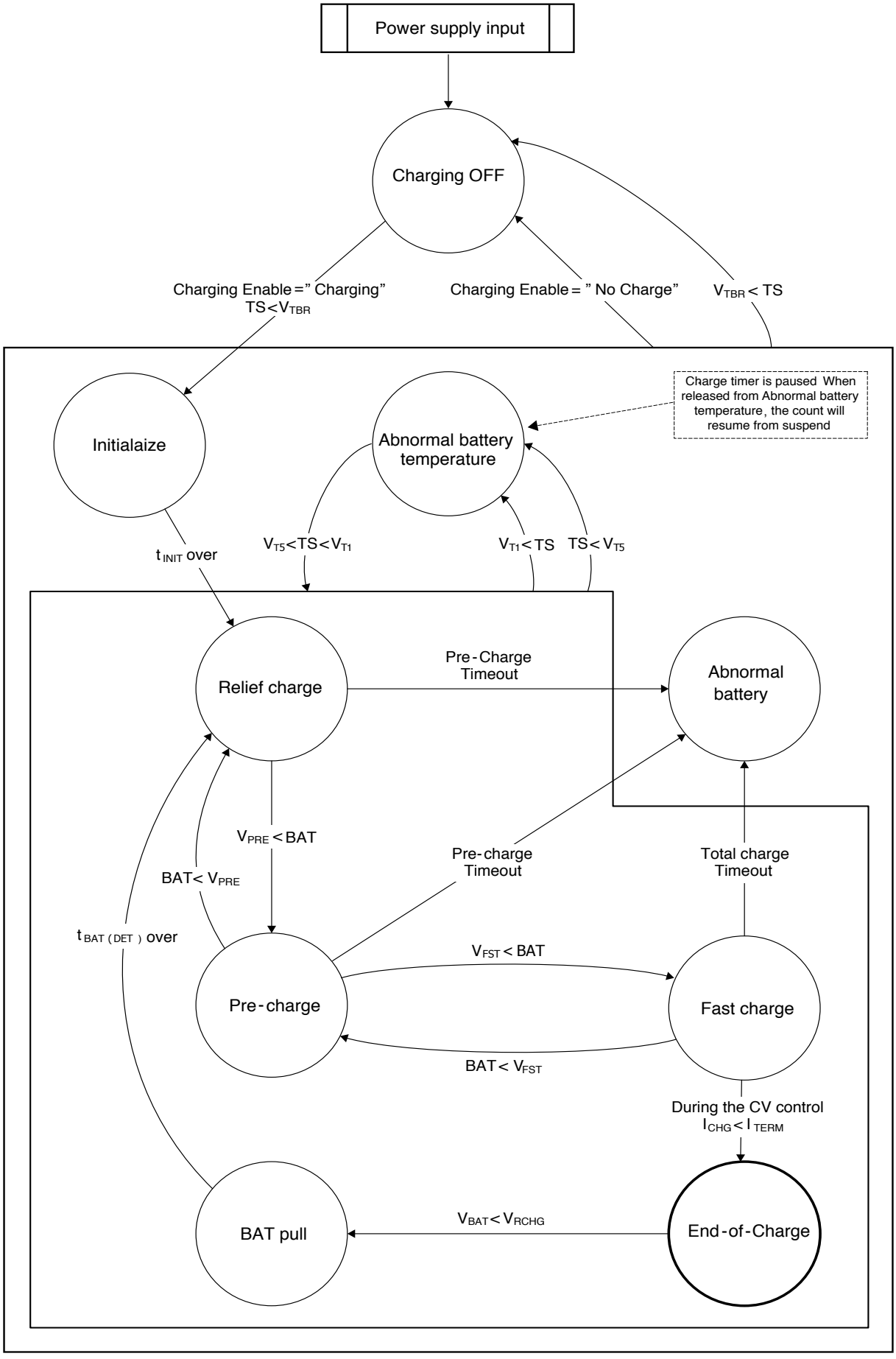
When Pre-charge timer or Total charge timer is time-up, remove power supply or remove battery or make ChargeEnable into “No charge” to reset.

CHG pin is NchMOS open drain output. While charging current is flowing, open drain MOS is turned on.

Charge Timing Chart



Charge State Machine



(12) CHARGE CURRENT LIMIT

When the sum total of OUT pin load current and charging current is larger than an input current limit, OUT pin voltage falls. If OUT pin voltage decreases from 4.2V (=VOUTBPM), charging current will be restricted and the fall of OUT pin voltage will be prevented. Charge status does not become full charge while this function is operating.

Even if the charging current limit function operates and it restricts charging current to 0mA, when OUT pin voltage continues falling, the battery support function operates.

(13) THERMAL REGULATION

If the chip temperature of MM3538 rises during charge operation and it becomes 100℃ (= Tj (REG)), charging current will be restricted and generation of heat will be prevented. Even if the thermal regulation function operates and it restricts charging current to 0mA, if chip temperature continues rising and chip temperature rises to 150℃ (= Tj (TSD)), the thermal shutdown function will operate.

(14) THERMAL SHUTDOWN

In order to protect MM3538 from thermal destruction, the thermal shutdown circuit is built in, and if chip temperature rises to 150℃ (=Tj(TSD)), it will be in a thermal shutdown state. A system-path is turn off, and a battery-path is turn ON during a thermal shutdown.

(15) CHARGE TIMER

For safety reservation of charge, MM3538 builds in the pre-charge timer and the total charge timer. judges with it being unusual with a timer passing the deadline of, and suspends charge. Charge is suspended when time-up happened. It is as follows during the count of each timer.

・Pre-charge timer：Relief charge + Pre-charge
・Total charge timer：Relief charge + Pre-charge + Fast charge

The clock frequency used by the pre-charge timer and a total charge timer is determined with the resistance of ISET pin and capacity of TMR pin.

$$T_{OSC}\,[s] = \frac{2 \cdot C_{TMR}\,[F]}{0.8\,[V] / R_{ISET}\,[\Omega]}$$

$$T_{BASE}\,[s] = T_{OSC}[s] \times 2^{20}$$

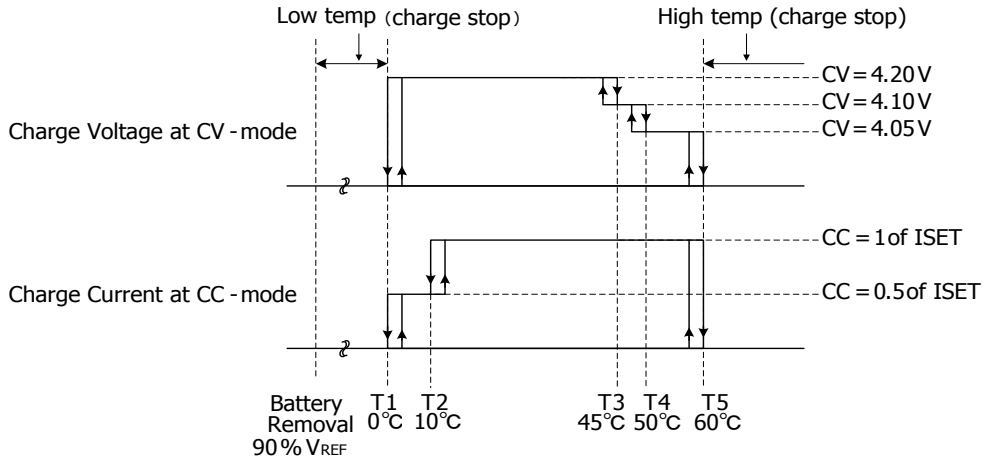
The time of a pre-charge timer and a total charge timer sets up what time of the obtained base frequency (= TBASE) is used by I2C (=I2C 05h b06~b01).

During fast charge, when charging current decreases by operation of a charging current limit function, in roportion to the reduction rate, a clock frequency becomes small. For example, when a fast charge current setup is 500mA and it decreases to 250mA by the above-mentioned factor, a clock frequency is set to one half and, as a result, the time of a charge timer doubles.

(16) CHARGE TEMPERATURE PROFILE

MM3538 corresponds to the charge temperature profile which JEITA recommends. Each CCCV value can be set up in four (T1~T2, T2~T3, T3~T4, and T4~T5) using I²C (=I²C 01h~03h). Moreover, MM3538 is optimized by the two following kinds of thermo sensitive registers, and can be chosen by I²C (=I²C 05h b07).

① NCP15WF104F03RC (100kohm, 4250K, Murata Manufacturing)
② NCP15XH103F03RC (10kohm, 3380K, Murata Manufacturing)



Example of charge temperature profile
(CCCV value of T1~T5 can be changed)

(17) SAL PIN

When the following factor occurs and the contents of the I^2C register change, a SAL terminal tells you. This pin is a NchMOS open drain output. When the contents of the I^2C register change, open drain MOS is turned on.

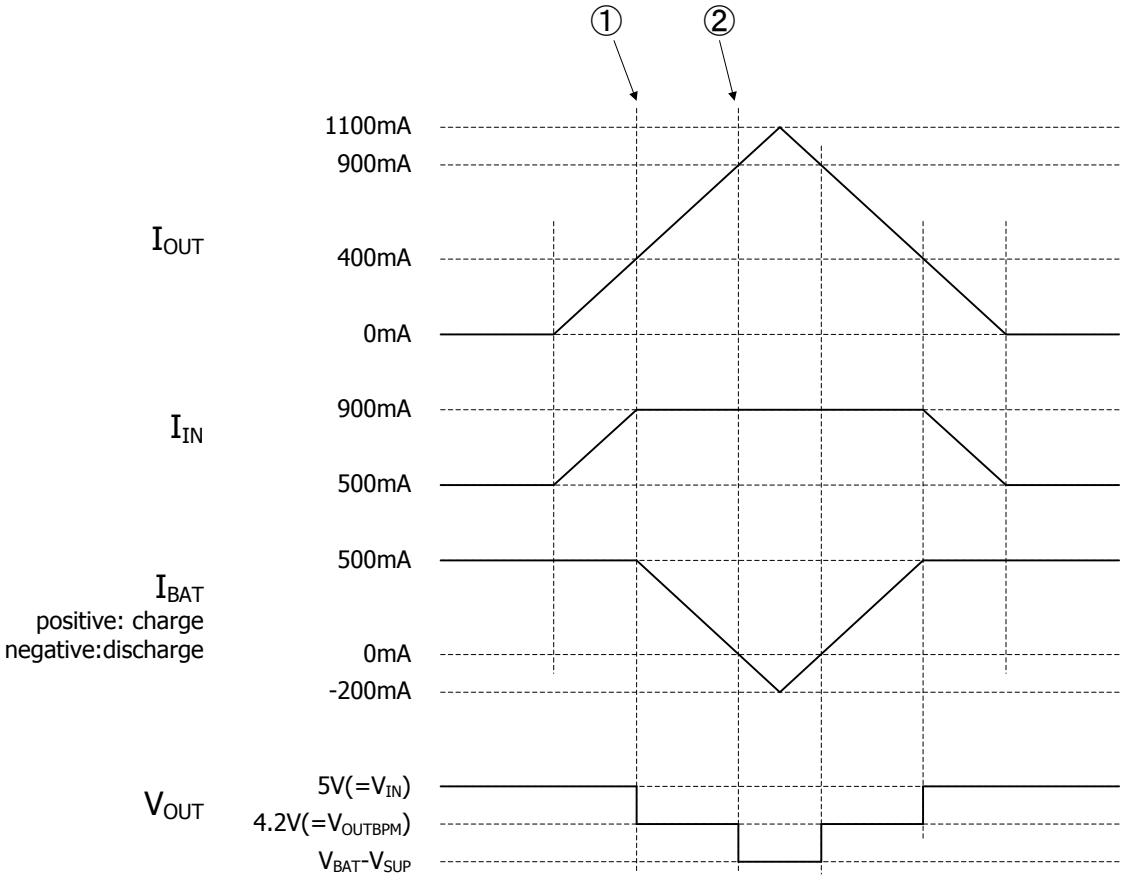
① When battery-temp becomes low-temp (~T1) or high-temp (T5~) (=I^2C 04h b07~b05)
② When pre-charge timer or total charge timer is time-up (=I^2C 04h b04)
③ Input overvoltage protection function operates (=I^2C 04h b03)
④ When ILIM pin short to GND (=I^2C 04h b02)
⑤ When ISET pin short to GND (=I^2C 04h b01)

After a SAL pin becoming "L", in order to return to H", it is necessary to control SAL Release (=I^2C 02h b00). While it has been in the state which the above-mentioned factor generated, even if it performs SAL Release, since there is no change in the contents of the I^2C register, a SAL pin does not react again.

(18) BATTERY SUPPORT

Although the current load of an OUT terminal is large and the charging current limit function is operating, a battery-path is turned on, if OUT terminal voltage continues falling and it falls from BAT-150~300mV(=V_{SUP}). By this, current will be supplied from both an input power source and a battery, and the fall of OUT terminal voltage is prevented. As an example, the timing chart at the time of the following setup is shown.

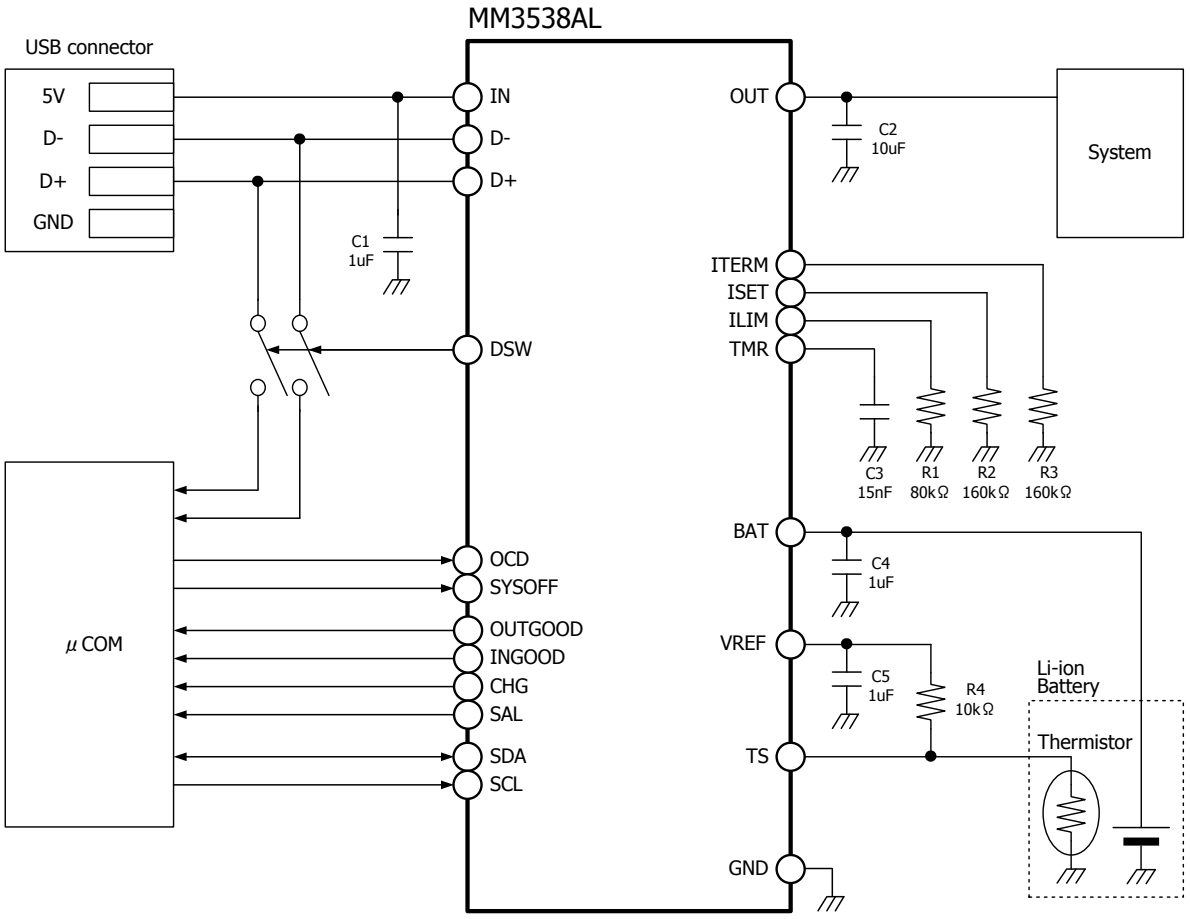
【 The example of a setting 】
Charge Current setting = 500mA
USB Current limit = 900mA (use ILIM pin)



The sum total of I_{OUT} and I_{BAT} becomes larger than 900mA, and V_{OUT} falls by an input limit function. Simultaneously, the charging current limit operates and charging current decreases so that V_{OUT} may not fall.

By a charging current limit function, even if it controls charging current to 0mA, when V_{OUT} falls, the battery support function operates and it prevents the fall of V_{OUT}.

Application Circuit



These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied.

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