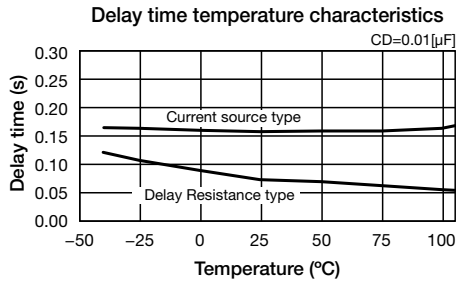
System Reset IC with delay
Monolithic IC PST89XB Series

Outline

This IC is a reset IC for turning on/off power supply and power flicker in CPU or logic systems.
This IC can change delay time by an external capacitor.
Charging method of the capacitor, is current source type.
Current source type can reduce temperature fluctuations in the delay time. td typ. ±6% (Ta=−40°C to 105°C), It is ideal for a wide set the operating temperature range.

Features

1.	Maximum supply voltage	7V
2.	Detecting voltage accuracy	±1.0%
3.	Low supply current	0.35μA typ.
4.	Operating supply voltage	0.95 to 6.5V
5.	Operating temperature	-40 to +105°C
6.	Reset voltage rank	1.6 to 5.2V (0.1Vstep)
7.	Reset temperature coefficient	±100ppm/°C typ.
8.	Current source	100nA typ.
9.	Output type	Open drain, CMOS



Packages

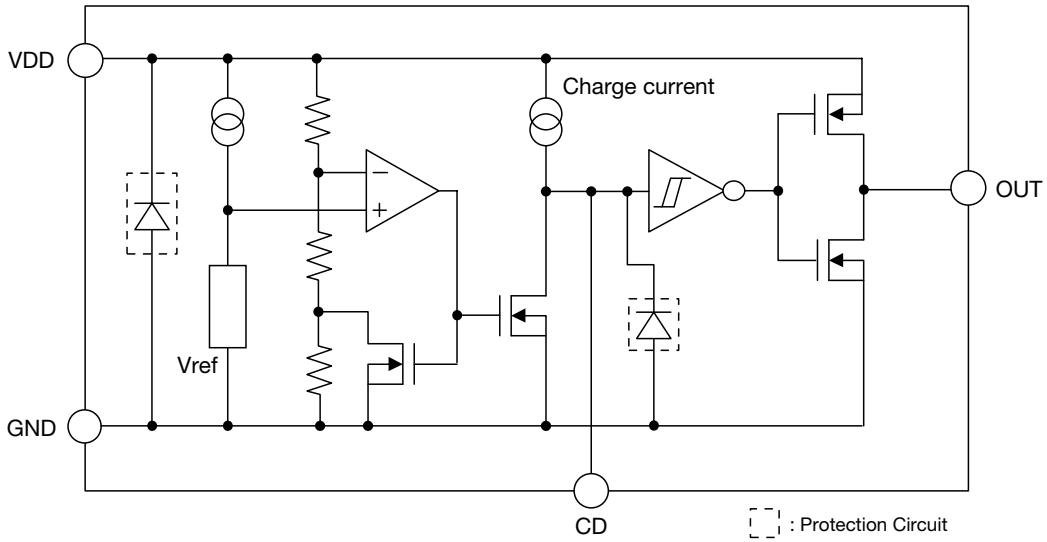
SC-82ABB
SOT-25A

Applications

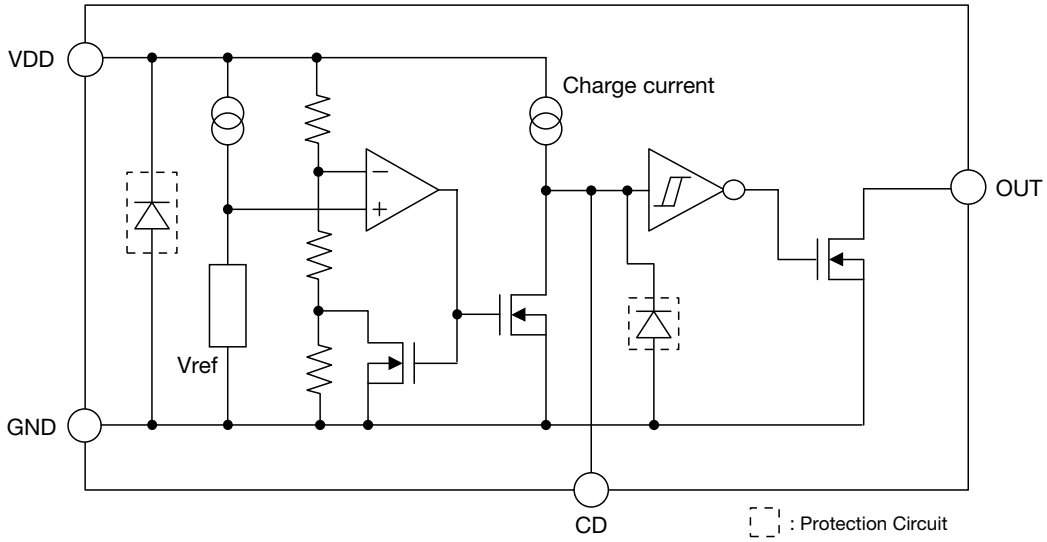
1. The reset of CPU and MPU and logic circuit
2. Battery voltage check
3. Back-up circuit
4. Level detector

Block Diagram

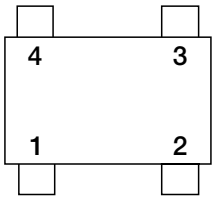
PST893Bxxx



PST894Bxxx

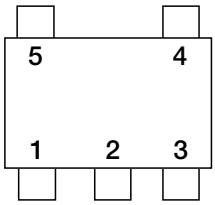


Pin Assignment



SC-82ABB
(TOP VIEW)

1	GND
2	VDD
3	CD
4	OUT



SOT-25A
(TOP VIEW)

1	OUT
2	VDD
3	GND
4	NC
5	CD

Pin Description

SC-82ABB

Pin No.	Pin name	Functions
1	GND	GND Pin
2	VDD	VDD Pin / Voltage Detect Pin
3	CD	Capacitor Connect Pin with Delay
4	OUT	Reset Signal Output Pin

SOT-25A

Pin No.	Pin name	Functions
1	OUT	Reset Signal Output Pin
2	VDD	VDD Pin / Voltage Detect Pin
3	GND	GND Pin
4	NC	No Connection
5	CD	Capacitor Connect Pin with Delay

Absolute Maximum Ratings (Except where noted otherwise Ta=25°C)

Item	Symbol	Ratings		Units
Supply Voltage	VDD max.	−0.3~+7.0		V
Output Voltage	OUT	PST893 Series	GND−0.3 ~ VDD max. +0.3	V
		PST894 Series	GND−0.3 ~+7.0	
Input Current (V_{DD})	I_{DD}	0~20		mA
Output Current (OUT)	I_{OUT}	0~20		mA
CD Pin Input Voltage	V_{CD}	GND−0.3 ~ VDD max. +0.3		V
Power dissipation	Pd	150		mW
Operating temperature	Topr	−40~+105		°C
Storage temperature	Tstg	−65~+125		°C

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating Ambient temperature	Topr	−40~+105	°C
Operating voltage	V_{DD}	0.95~6.5	V

Model Name

P S T 8 9 □ B □ □ □ □ □

a b c d e

a		b		c		d		e	
Output Type		CD pin charge Type		Detecting Voltage Rank		Package		Packing Specifications	
3	CMOS Output	B	Current source	160	Setting of the detection voltage from 1.6V to 5.2V,0.1V step.	U	SC-82ABB	M	R HOUSING Halogen-free Product
4	Open drain Output			≀		N	SOT-25A	H	L HOUSING Halogen-free Product
				520					

Electrical Characteristics (Except where noted otherwise Ta=25°C)

Item	Symbol	Measurement conditions	Rank	Min.	Typ.	Max.	Units	Circuit
Reset threshold (Note1)	V_{TH}	Ta=+25°C Ta=−40~+85°C	160	1.5840	1.6000	1.6160	V	2
				1.5600		1.6400		
			170	1.6830	1.7000	1.7170		
				1.6575		1.7425		
			180	1.7820	1.8000	1.8180		
				1.7550		1.8450		
			190	1.8810	1.9000	1.9190		
				1.8525		1.9475		
			200	1.9800	2.0000	2.0200		
				1.9500		2.0500		
			210	2.0790	2.1000	2.1210		
				2.0475		2.1525		
			220	2.1780	2.2000	2.2220		
				2.1450		2.2550		
			230	2.2770	2.3000	2.3230		
				2.2425		2.3575		
			240	2.3760	2.4000	2.4240		
				2.3400		2.4600		
			250	2.4750	2.5000	2.5250		
				2.4375		2.5625		
			260	2.5740	2.6000	2.6260		
				2.5350		2.6650		
			270	2.6730	2.7000	2.7270		
				2.6325		2.7675		
			280	2.7720	2.8000	2.8280		
				2.7300		2.8700		
			290	2.8710	2.9000	2.9290		
				2.8275		2.9725		
			300	2.9700	3.0000	3.0300		
				2.9250		3.0750		
			310	3.0690	3.1000	3.1310		
				3.0225		3.1775		
			320	3.1680	3.2000	3.2320		
				3.1200		3.2800		
			330	3.2670	3.3000	3.3330		
				3.2175		3.3825		
			340	3.3660	3.4000	3.4340		
				3.3150		3.4850		
			350	3.4650	3.5000	3.5350		
				3.4125		3.5875		
			360	3.5640	3.6000	3.6360		
				3.5100		3.6900		
			370	3.6630	3.7000	3.7370		
				3.6075		3.7925		
			370	3.7620	3.8000	3.8380		
				3.7050		3.8950		
			390	3.8610	3.9000	3.9390		
				3.8025		3.9975		
			400	3.9600	4.0000	4.0400		
				3.9000		4.1000		

Note1 : This device is tested at Ta=25℃, over temperature limits guaranteed by desigh only.
Note2 : The parameter is guaranteed by design.

Item	Symbol	Measurement conditions	Rank	Min.	Typ.	Max.	Units	Circuit
Reset threshold (Note1)	V_{TH}	Ta=+25°C Ta=−40~+85°C	410	4.0590	4.1000	4.1410	V	2
				3.9975		4.2025		
			420	4.1580	4.2000	4.2420		
				4.0950		4.3050		
			430	4.2570	4.3000	4.3430		
				4.1925		4.4075		
			440	4.3560	4.4000	4.4440		
				4.2900		4.5100		
			450	4.4550	4.5000	4.5450		
				4.3875		4.6125		
			460	4.5540	4.6000	4.6460		
				4.4850		4.7150		
			470	4.6530	4.7000	4.7470		
				4.5825		4.8175		
			480	4.7520	4.8000	4.8480		
				4.6800		4.9200		
			490	4.8510	4.9000	4.9490		
				4.7775		5.0225		
			500	4.9500	5.0000	5.0500		
				4.8750		5.1250		
			510	5.0490	5.1000	5.1510		
				4.9725		5.2275		
			520	5.1480	5.2000	5.2520		
				5.0700		5.3300		

Note1 : This device is tested at Ta=25℃, over temperature limits guaranteed by desigh only.
Note2 : The parameter is guaranteed by design.

Item	Symbol	Measurement conditions	Rank	Min.	Typ.	Max.	Units	Circuit
Reset threshold hysteresis	ΔV_{TH}	V_{DD}=0V→V_{TH}+1V→0V	160	0.048	0.080	0.128	V	2
			170	0.051	0.085	0.136		
			180	0.054	0.090	0.144		
			190	0.057	0.095	0.152		
			200	0.060	0.100	0.160		
			210	0.063	0.105	0.168		
			220	0.066	0.110	0.176		
			230	0.069	0.115	0.184		
			240	0.072	0.120	0.192		
			250	0.075	0.125	0.200		
			260	0.078	0.130	0.208		
			270	0.081	0.135	0.216		
			280	0.084	0.140	0.224		
			290	0.087	0.145	0.232		
			300	0.090	0.150	0.240		
			310	0.093	0.155	0.248		
			320	0.096	0.160	0.256		
			330	0.099	0.165	0.264		
			340	0.102	0.170	0.272		
			350	0.105	0.175	0.280		
			360	0.108	0.180	0.288		
			370	0.111	0.185	0.296		
			380	0.114	0.190	0.304		
			390	0.117	0.195	0.312		
			400	0.120	0.200	0.320		
			410	0.123	0.205	0.328		
			420	0.126	0.210	0.336		
			430	0.129	0.215	0.344		
			440	0.132	0.220	0.352		
			450	0.135	0.225	0.360		
			460	0.138	0.230	0.368		
			470	0.141	0.235	0.376		
			480	0.144	0.240	0.384		
			490	0.147	0.245	0.392		
			500	0.150	0.250	0.400		
			510	0.153	0.255	0.408		
			520	0.156	0.260	0.416		

Note1 : This device is tested at Ta=25℃, over temperature limits guaranteed by desigh only.
Note2 : The parameter is guaranteed by design.

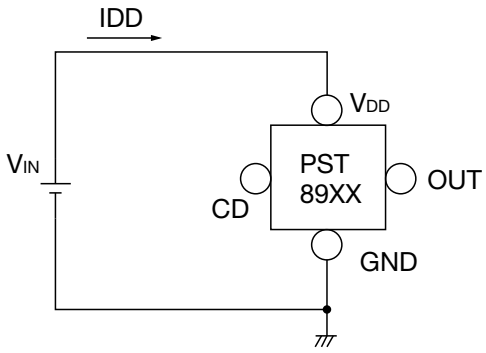
Item	Symbol	Measurement conditions	Rank	Min.	Typ.	Max.	Units	Circuit
Supply Current	I_{DD}	$V_{DD}=V_{TH}+1V$	160 ~ 520		0.35	1.0	µA	1
Reset threshold temp. coefficient (Note1)	$\Delta V_{TH}/°C$	Ta=–40~+85°C	160 ~ 520		±100		ppm/℃	2
L transfer delay time (Note2)	t_{PHL}	$V_{DD}=V_{TH}+0.4V$ →$V_{TH}-0.4V$	160 ~ 520	2	15	100	µs	6
H transfer delay time (Note2)	t_{PLH}	$V_{DD}=V_{TH}+0.4V$ →$V_{TH}-0.4V$	160 ~ 520	2	15	100	µs	6
"L" Output Current	I_{OL1}	$V_{DD}=0.95V$, $V_{DS}=0.05V$	160 ~ 520	0.01	0.10		mA	3
	I_{OL2}	$V_{DD}=1.2V$, $V_{DS}=0.5V$	160 ~ 520	0.23	2.00			
	I_{OL3}	$V_{DD}=2.4V$, $V_{DS}=0.5V$ $V_{TH}\geqq 2.5V$	250 ~ 520	1.60	8.00			
	I_{OL4}	$V_{DD}=3.6V$, $V_{DS}=0.5V$ $V_{TH}\geqq 3.7V$	370 ~ 520	3.20	12.0			
"H" Output Current	I_{OH1}	$V_{DD}=4.8V$, $V_{DS}=0.5V$ $V_{TH}\leqq 4.7V$ PST893 series only	160 ~ 470	0.36	0.62		mA	3
	I_{OH2}	$V_{DD}=6.1V$, $V_{DS}=0.5V$ PST893 series only	160 ~ 520	0.46	0.75			
Output Leakage Current	Ileak	$V_{DD}=6.5V$, OUT=6.5V PST894 series only	160 ~ 520			0.1	µA	3
CD Pin charge Current	I_D	$V_{DD}=V_{TH}+1V$ $V_{DS}=0V$	160 ~ 520	90	100	110	nA	5
CD Pin Threshold Voltage	V_{TCD}	$V_{DD}=V_{TH}\times 1.1V$	160 ~ 520	VDD×0.3	VDD×0.5	VDD×0.7	V	4
CD Pin Output Current1	$I_{CD}1$	$V_{DD}=0.95V$ $V_{DS}=0.1V$	160 ~ 520	2.0	30.0		µA	5
CD Pin Output Current2	$I_{CD}2$	$V_{DD}=1.5V$ $V_{DS}=0.5V$	160 ~ 520	200	800		µA	5

Note1 : This device is tested at Ta=25℃, over temperature limits guaranteed by desigh only.

Note2 : The parameter is guaranteed by design.

Test Circuit

(1)



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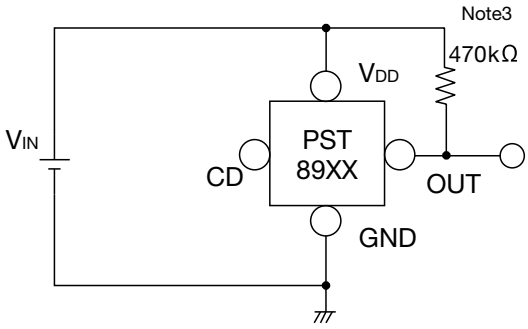

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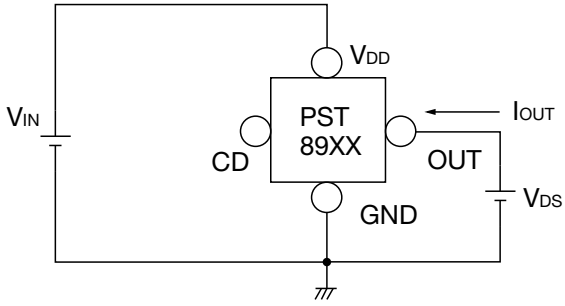

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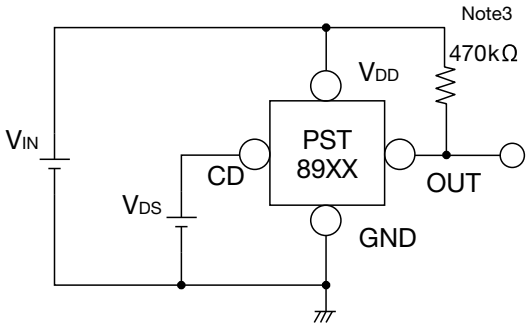

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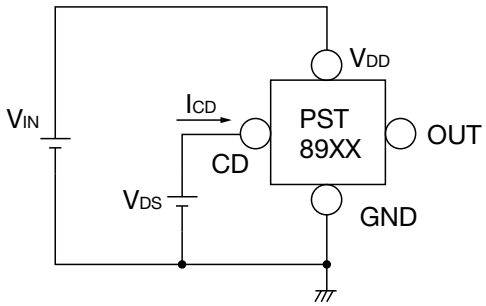

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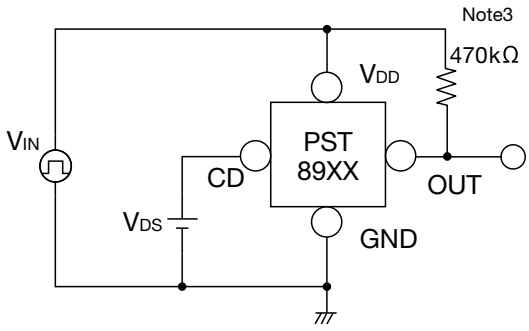
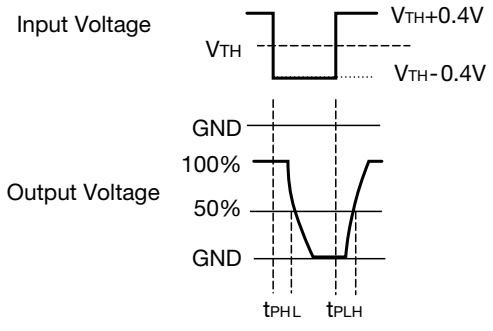
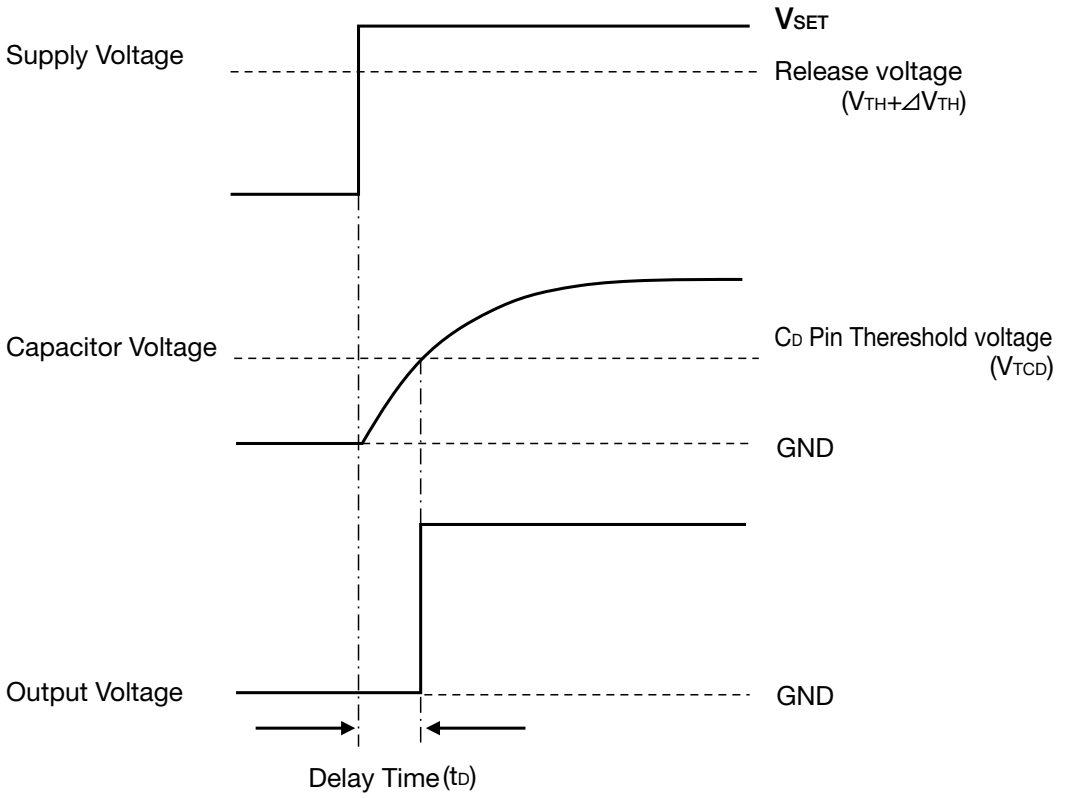




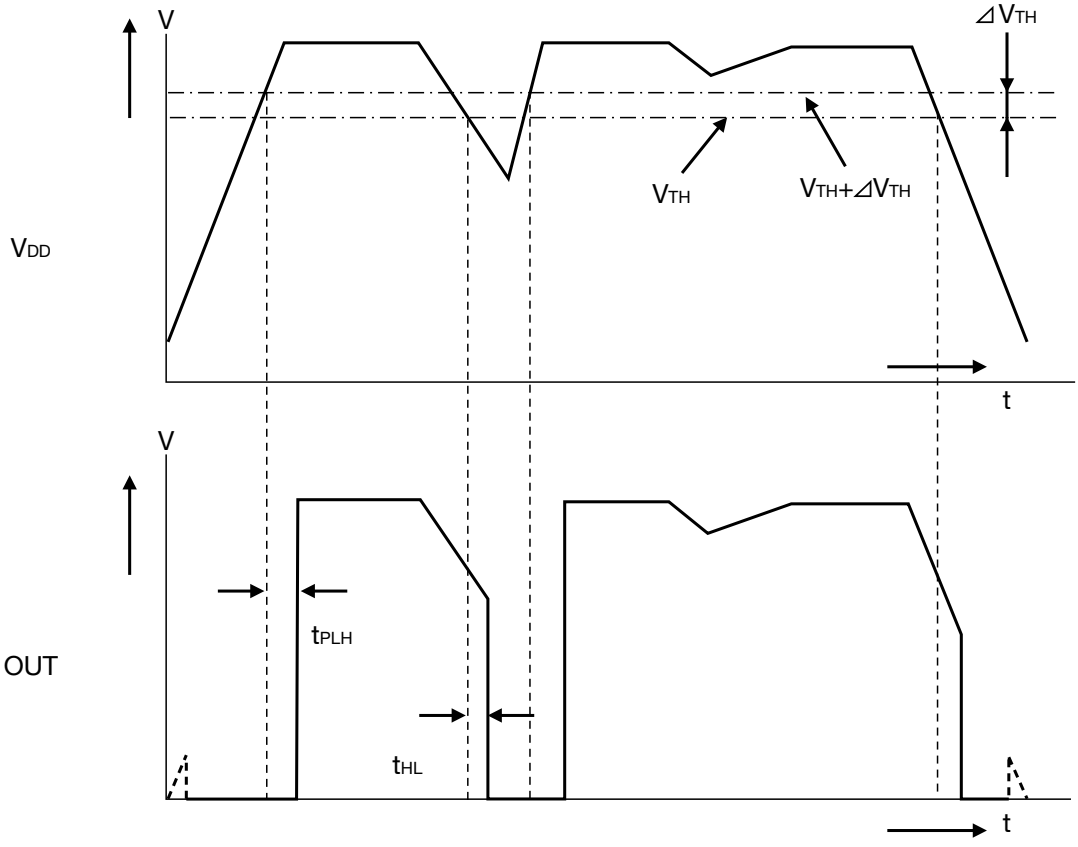
Note3 : PST894series only

Timing Chart



$t_D = C \times 0.5 \times V_{SET} / I_D$ (s)

C_D : Capacitor
V_{SET} : Supply voltage
I_D : C_D Pin Charge current 100nA. typ



Operation Explanation

· Detection Voltage
Refers to the VDD voltage when the voltage of the OUT terminal voltage switches from H level to L level when reducing the VDD voltage.

· Release Voltage
Refers to the VDD voltage when the voltage of the OUT terminal voltage switches from L level to H level when raising the VDD voltage.

· Hysteresis Voltage
Hysteresis voltage = release voltage - detection voltage, and refers to the difference in voltage.

· L Propagation Delay Time
Refers to the time from when the VDD voltage decreases below the detection voltage to when the OUT terminal voltage switches from H level to L level, and is the response time within the reset IC when a reduction in the supply voltage is detected.

· H Propagation Delay Time
Refers to the time from when the VDD voltage decreases below the release voltage to when the OUT terminal voltage switches from L level to H level, and is the response time within the reset IC when the power supply starts up.

· Release Delay Time
Refers to the delay time for switching the OUT terminal during the condenser charging time due to the CD terminal condenser and charging current within the reset IC.
Configured with the time or delay until voltage stabilizes when the set power supply starts up.

· ”L” Output Current
Drain current of the OUT terminal NMOS. The synchronization current that turns the NMOS ON and sets the OUT terminal voltage to L level when VDD < detection voltage. Select the appropriate pull-up resistance for the synchronization capability for open drain output parts. If the pull-up resistance value is too low, VDS is generated so that L level voltage ≒ 0.3V, and may not reach ≒ 0V.

· ”H” Output Current
The drain current of the OUT terminal PMOS for CMOS output parts. The synchronization current that turns the PMOS ON and sets the OUT terminal voltage to H level when VDD > release voltage.

· Delay Terminal Charging Current
Refers to the current for charging the condenser connected to the CD terminal to generate the release delay time.

· Delay Terminal Threshold Value Voltage
Refers to the CD terminal voltage refers to the threshold voltage that is input into subsequent inverters to reverse the inverter output.

· Delay Terminal Output Current
The drain current of the CD terminal NMOS. Refers to the current for charging the condenser connected to the CD terminal.
As the discharge current capability is small at around several 100 μA, a delay is generated for the OUT terminal response time corresponding to the discharge time as the CD terminal capacity value increases. Check operation when the delay is 1μF or more in particular.

· Delay Terminal
The delay terminal is the current source and has a high impedance. If board leakage, condensation or other leakages occur at the CD terminal, logical inversion occurs at subsequent inverters and logical inversion also occurs at the OUT terminal.
The delay terminal has a high impedance and logical inversion may occur due to factors such as external noise, so using the terminal while OPEN is not recommended.
Use the delay terminal by connecting it with 100 pF or more.

For the setting of the release delay time

- **Operation of the power supply start-up**

1 It raised to VDD = 0V → VSET.

2 Comparator to detect release voltage (detection voltage + hysteresis voltage) or more.

3 Discharge NMOS of the CD pin : ON → OFF.
It is charged the capacitor of the CD pin from delay pincharge current.

4 Capacitor of the CD pin is charged, the inverter detects the above "0.5×VDD".
The threshold voltage of the inverter is the following.
CD Pin Threshold Voltage VDD×0.3min. -VDD×0.5typ. -VDD×0.7max

5 OUT : L → H, it is released from the reset.

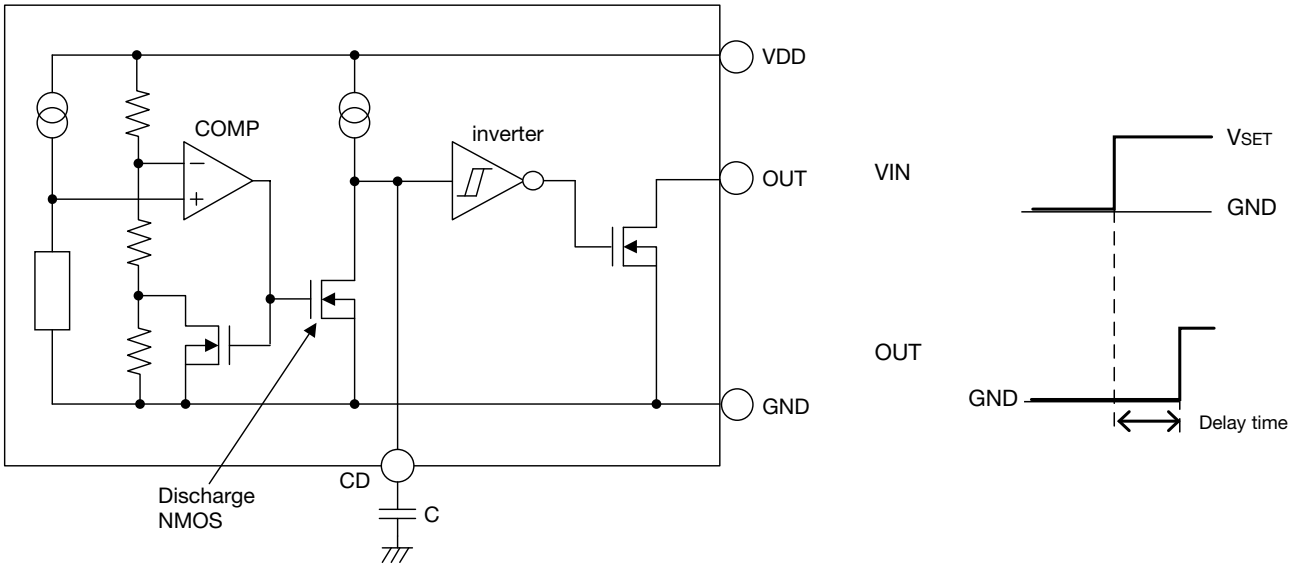
- **For the setting of the release delay time PST89xB series**

A constant current source, relationship charging time of the capacitor $Q=I\times t=C\times V$

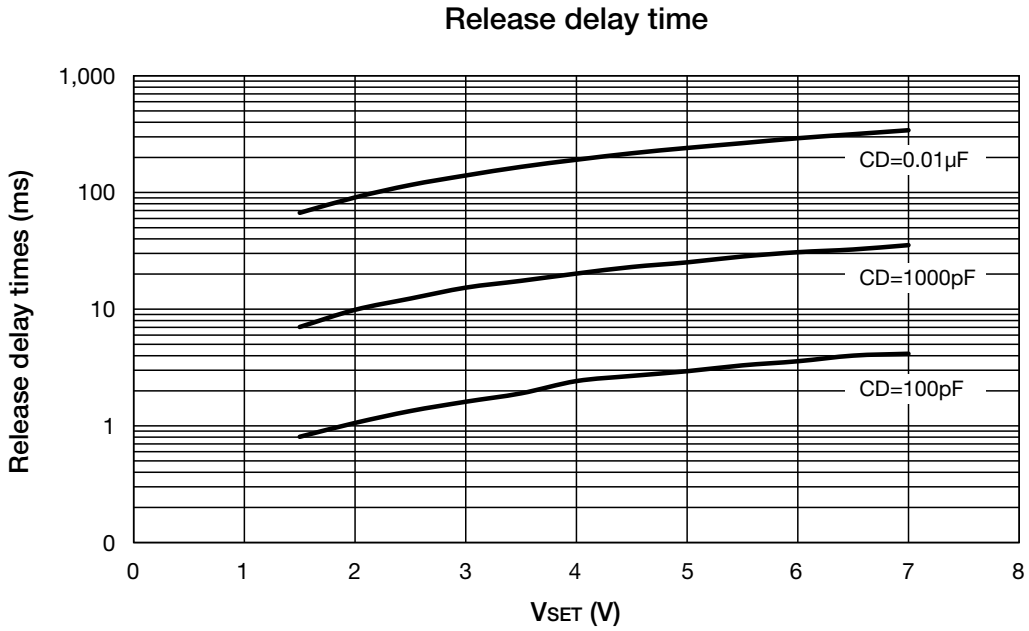
Release delay time, it is time to be "CD Pin Voltage" = "the threshold voltage of the inverter"
VTCD typ = 0.5×VSET ".
It will be prompted by the following equation.

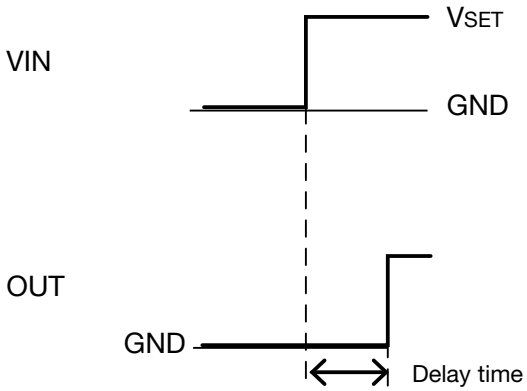
$t_{D\,typ} = C\times V_{TCD\,typ} / I_D = C\times 0.5\times V_{SET} / I_D$ (s)

C_D : Capacitor
V_{SET} : Supply voltage
I_D : CD pin charge current 100nA typ.

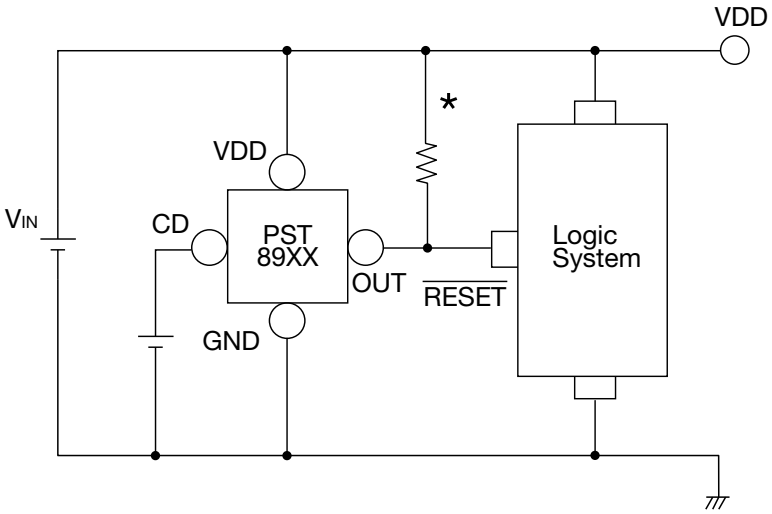


- PST89xB series release delay time TYPICAL PERFORMANCE CHARACTERISTICS

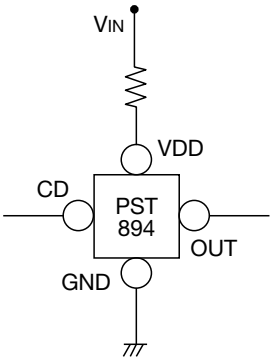


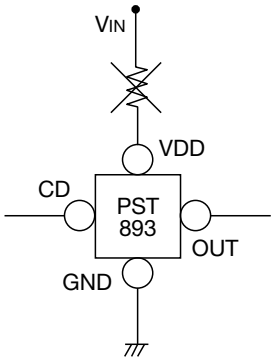


Application Circuits



* PST894 Series only

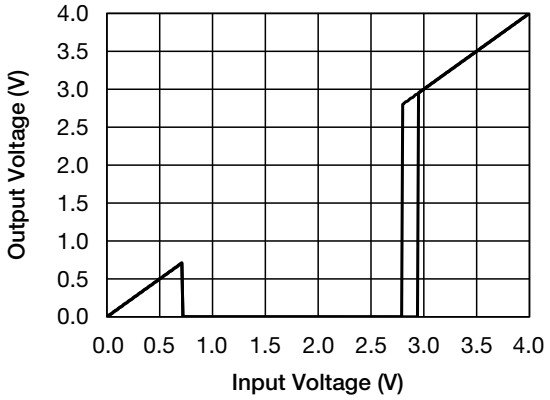




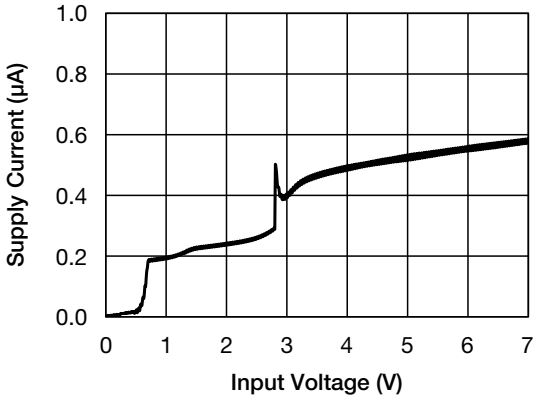
- We shall not be liable for any trouble or damage caused by using this circuit.
- In the event a problem which may affect industrial property or any other rights of us or a third party is encountered during the use of information described in these circuit, Mitsumi Electric Co., Ltd. shall not be liable for any such problem, nor grant a license therefore.
- Please note that there is any possibility of circuit oscillation when resistance put in the line VIN. Recommend 15k ohm or less for PST894.
  Please do not put resistance for PST893.
- TYP hysteresis voltage of PST89 series is a detecting voltage × 0.05.
  During power-up, and to release reset, it is time that it has become more than the release voltage (= detection voltage + hysteresis voltage).
  By calculating the variation of the power supply and the detection voltage and the release voltage, please select the detecting voltage rank.
- In CD pin, please do not use from the external voltage, and current source.
- Between CD pin ~ GND pin, please use by connecting more than capacitor 100pF.
- When the CD terminal capacitance value is greater than or more 1μF, time of the charge and discharge, the response of the OUT waveform is delayed.
  To power reduction of short-pulse, and less likely to respond.
  By the power supply voltage drop due to instantaneous interruption, the ack of discharge current capability of CD terminal, is not completely discharge, increasing again power-than release delay time of setting, it will be shorter.

Characteristics (2.8V) (Except where noted otherwise Ta=25°C)

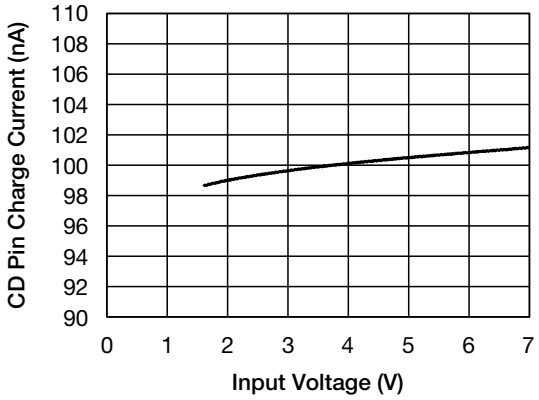
Detecting Voltage



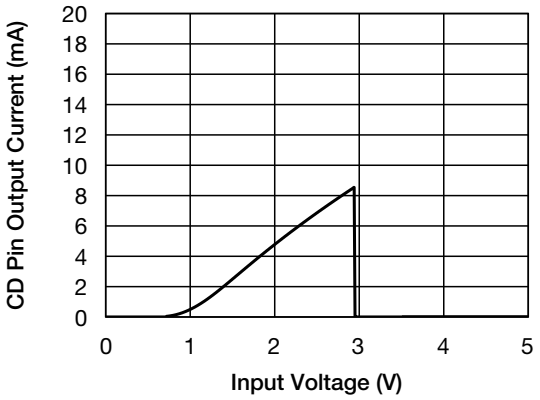
Supply Current



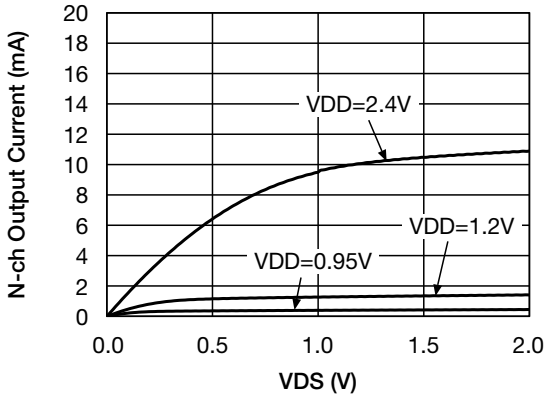
CD Pin Charge Current



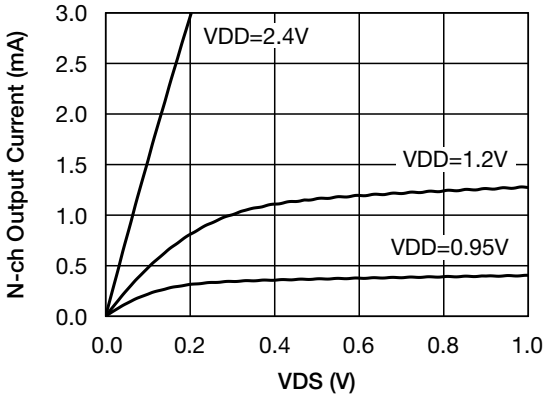
CD Pin Output Current



N-ch Output Current

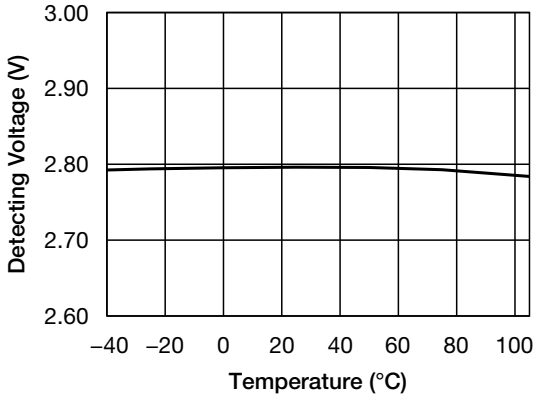


N-ch Output Current

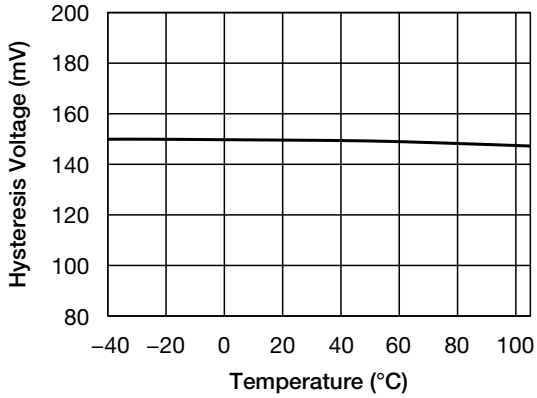


Note : * These are typical characteristics.

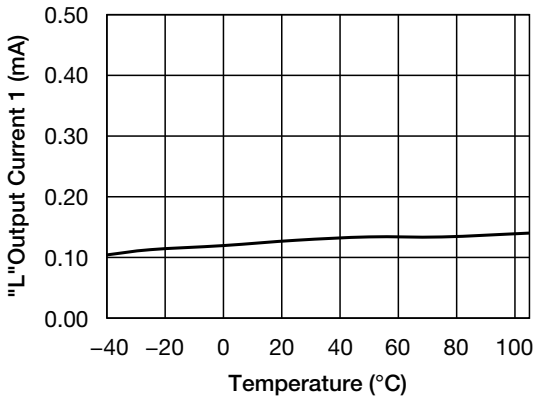
Detecting Voltage - Temperature



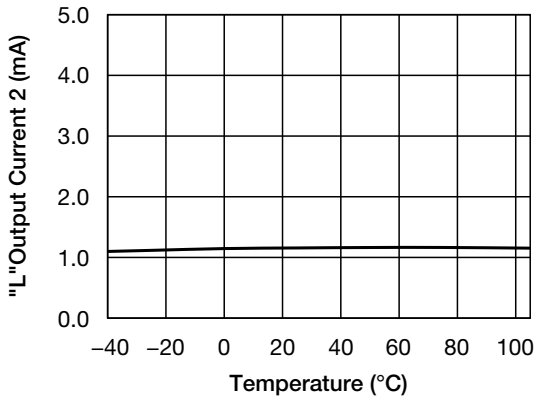
Hysteresis Voltage - Temperature



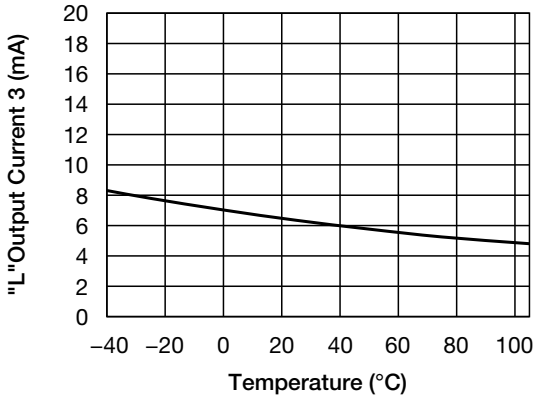
"L"Output Current 1 - Temperature



"L"Output Current 2 - Temperature

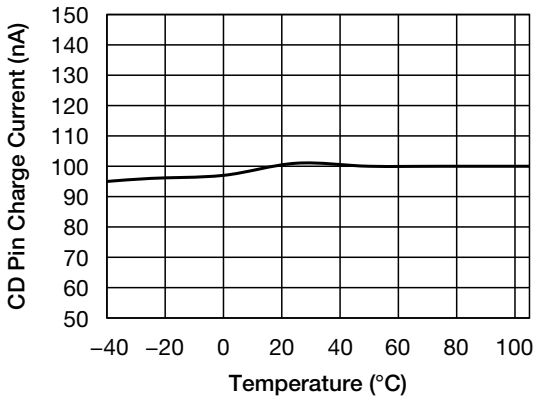


"L"Output Current 3 - Temperature

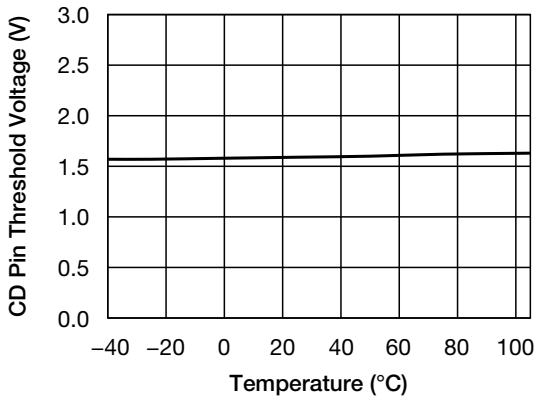


Note : * These are typical characteristics.

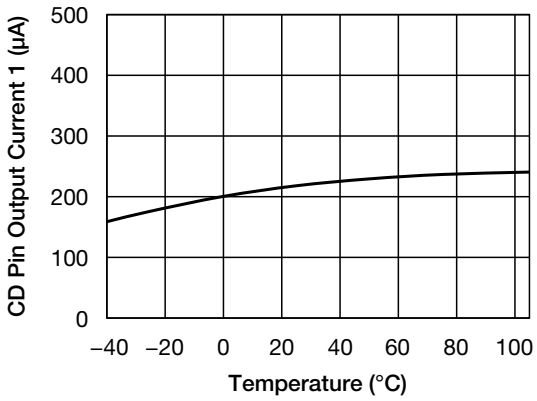
CD Pin Charge Current – Temperature



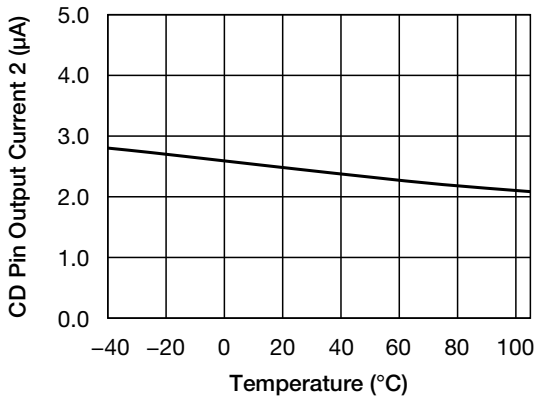
CD Pin Threshold Voltage – Temperature



CD Pin Output Current 1 – Temperature



CD Pin Output Current 2 – Temperature



Note : * These are typical characteristics.