2ch Synchronous Step-down DC/DC Converter + 1ch LDO + 2ch P-GOOD Monolithic IC MM3558 Series

Outline

This IC is a compound power supply IC which built in Synchronous Step-down DC/DC converter 2ch, LDO1ch, and P-GOOD2ch.

The ripple of the input current is decreased so that the DC/DC converter of 2ch may work by the opposite phase, and a low noise is achieved. Because the output voltage can be set by external resistance, it is possible to use it according to various output conditions.

Features

1. Input Operating Voltage Range	3.0V~5.5V	
2. Shutdown Supply Current	0.1µA (Typ.)	
3. Temperature Range	−30~+85°C	
4. DC/DC converters		
Output Voltage	1.0V~PVIN	Accuracy ±2%
Maximum Output Current	1.5A / 1ch	
Oscillator Frequency	2MHz (Typ.)	
Output Voltage is changeable in external parts.		
Built-in start/stop sequence circuit.		
Output OverVoltage Protection function	0.72V (Typ.)	
Built-in SoftStart circuit	1.5ms (Typ.)	
Built-in OverCurrent detection timer	1.5ms (Typ.)	
5. LDO		
Output Voltage	3.3V	Accuracy ±1%
Dropout voltage	0.10V (Typ.)	
Current limit	40mA (Typ.)	
6. P-GOOD		

Input/Output Over Voltage/Low Voltage, Over Current, and Thermal detection.

Package

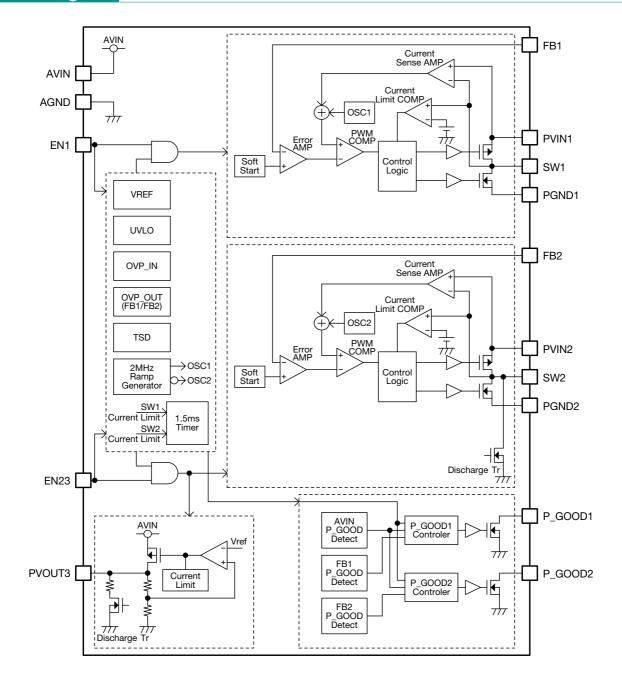
SQFN-16A

Applications

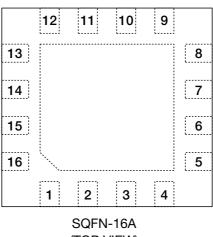
- 1. Printer
- 2. Composit device

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Block Diagram



Pin Assignment



(TOP VIEW)

1	P_GOOD2	9	PGND2
2	EN1	10	SW2
3	SW1	11	EN23
4	PGND1	12	P_GOOD1
5	FB1	13	PVIN2
6	TP	14	AVIN
7	PVOUT3	15	AGND
8	FB2	16	PVIN1

Pin Description

Pin No.	Pin name	Pin description	Internal equivalent circuit diagram
1 12	P_GOOD2 P_GOOD1	Power Good output pin	
2 11	EN1 EN23	Enable pin for ON/OFF	AVIN W AGND
3 10	SW1 SW2	Power switched pin	PVIN —I Bischarge Tr SW2 Only —I PGND PGND
4 9 15	PGND1 PGND2 AGND	Ground pin	PGND
5 8	FB1 FB2	DC/DC output voltage feedback pin	AVIN Err Amp AGND
6	TP	Test pin (Please connect with GND.)	AVIN AVIN AGND

Pin No.	Pin name	Pin description	Internal equivalent circuit diagram
7	PVOUT3	Regulator output pin	AVIN HE AGND PGND
13 16	PVIN2 PVIN1	Power supply input pin	PVIN Intenal Circuit PGND
14	AVIN	Power supply input pin	AVIN Intenal Circuit AGND

Absolute Maxim	um Ratings	(Except where noted otherwise Ta=25°C)
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Item	Symbol	Ratings	Units
AVIN Voltage	VAVIN	-0.3~+6.0	V
PVIN1 Voltage	V _{PVIN1}	-0.3~+6.0	V
PVIN2 Voltage	V _{PVIN2}	-0.3~+6.0	V
SW1 Voltage	Vsw1	-0.6~Vpvin1+0.3	V
SW2 Voltage	Vsw2	-0.6~Vpvin2+0.3	V
FB1 Voltage	VFB1	-0.3~+6.0	V
FB2 Voltage	V_{FB2}	-0.3~+6.0	V
P_GOOD1 Voltage	V _{PG1}	-0.3~+6.0	V
P_GOOD2 Voltage	VPG2	-0.3~+6.0	V
EN1 Voltage	Ven1	-0.3~+6.0	V
EN23 Voltage	VEN23	-0.3~+6.0	V
PVOUT3 Voltage	VPVO3	-0.3~VAVIN+0.3	V
SW1 Maximum Current	Isw1	1.8	A
SW2 Maximum Current	Isw2	1.8	A
P_GOOD1 Maximum Current	IPG1	200	mA
P_GOOD2 Maximum Current	IPG2	200	mA
PVOUT3 Maximum Current	IPV03	50	mA
Storage Temperature	Tstg	-55~+150	°C
Power Dissipation (Alone)	PD	220 (Note1)	mW

Note1 : The values indicate reference values.

Recommended Operating Conditions (Except where noted otherwise Ta=25°C)

Item	Symbol	Ratings	Units
AVIN Voltage	VAVIN	3.0~5.5	V
PVIN1 Voltage	VPVIN1	3.0~5.5	V
PVIN2 Voltage	V_{PVIN2}	3.0~5.5	V
SW1 Current	Isw1	0~1.5	А
SW2 Current	Isw2	0~1.5	А
DC/DC Converter Output Voltage (Note2)	Vdco	1.0~PVIN	V
PVOUT3 Current	IPV03	0~10	mA
Operating Temperature	Topr	-30~+85	°C
Junction Temperature (Note3)	TJ	150	°C

Note2 : There is a case to take operation from 1 to 2 when applying to the following condition in addition to the thing without the voltage difference between the input and the output.

- · Duty 90% or more
- \cdot Hiside Tr ON resistance \times load current > voltage difference between the input and the output
- 1) If Duty becomes 100%, the output voltage decreases depending on "Input voltage- Hiside Tr ON resistance × load current".
- 2) There is a case that becomes operation that the switching operates at a cycle different from the oscillatory frequency that looks like the abnormally oscillation.
- Note3: Please calculate TJ from ambient temperature TA and power consumption Preferring to the next expression.

 $TJ = TA + P \times 62.2 \text{°C/W}$

Thermal resistance 62.2 °C/W is a value when the substrate size mounts on two glass epoxy layer substrate of $90 \times 90 \times 1.6$ mm³ (copper interconnect rate 90%).

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Electrical Characteristics

(Except where noted otherwise AVIN=PVIN1=PVIN2=5.0V, EN1=EN23=5.0V, Ta=25°C)

Item	Symbol	Measurement conditions	Min.	Тур.	Max.	Units	Measuring Circuit No.
Supply Current1 (DCDC1)	I _{DD1}	EN1=5V, EN23=0V FB1=0.65V		350	525	μA	2
Supply Current2 (DCDC2, PVOUT3)	I_{DD2}	EN1=0V, EN23=5V FB2=0.65V		400	600	μA	2
Supply Current (No switching)	I_{DD3}	FB1=FB2=0.55V PVOUT3=No Load		600	900	μA	2
Shutdown Current	I _{OFF}	EN1=EN23=0V		0.1	1.0	μA	2
VIN UVLO Detection Voltage	V _{UVLOD}	AVIN=4.5V→0V	2.45	2.55	2.65	V	2
VIN UVLO Release Voltage	V _{UVLOR}	AVIN=0V→4.5V	V _{UVLOD} +100	V _{UVLOD} +150	V _{UVLOD} +200	mV	2
OVP_IN Detection Voltage	V _{OVPID}	AVIN=5.0V→6.0V	5.6	5.8	6.0	v	2
OVP_IN Release Voltage	V _{OVPIR}	AVIN=6.0V→5.0V		V _{ovpid} -150		mV	2
OVP_OUT Detection Voltage	V _{OVPOD}	FB1(FB2)=0.6→0.8V	0.66	0.72	0.76	V	2
OVP_OUT Release Voltage	V _{OVPOR}	FB1(FB2)=0.8→0.6V		V _{OVPOD} -25		mV	2
EN1, EN23 pin "High" Input Voltage	V _{ENH}		AVIN/2			V	2
EN1, EN23 pin "Low" Input Voltage	V _{ENL}				0.5	V	2
EN1, EN23 Pin Input Current	I _{EN}	EN=6V		2		μA	2
Thermal Shutdown Detection	V _{THD}	No switching		150		°C	
Thermal Shutdown Release	V _{THR}	No switching		120		°C	
DC/DC converter							
FB1, 2 Voltage	$V_{\rm FBPWM}$	VOUT=1.8V L=2.7µH, COUT=22µF	0.588	0.600	0.612	v	1
FB1, 2 Pin Current	\mathbf{I}_{FB}	FB1=FB2=6V	-1.0		+1.0	μA	2
Oscillator Frequency	f _{OSC}		1.8	2.0	2.2	MHz	1
Hiside Tr Current Limit (Note4)	I _{LIMSW}		1.7		3.0	A	1
Hiside Tr ON Resistance	R _{SWH}	SW1(SW2)=100mA sink		0.3	0.6	Ω	2
Lowside Tr ON Resistance	R _{SWL}	SW1(SW2)=100mA source		0.25	0.5	Ω	2
Soft Start Time	t _{ss}	Time till it reaches to FB×0.9	0.5	1.5	2.5	ms	1
SW2 Pin Discharge Tr ON Resistance	R _{DSW2}	EN23=0V SW2=5.0V		100		Ω	2

Note4 : The parameter is guaranteed by design.

Item	Symbol	Measurement conditions	Min.	Тур.	Max.	Units	Measuring Circuit No.
Regulator							
PVOUT3 Output Voltage 1	V _{VO31}	PVOUT3=No load	3.267	3.300	3.333	V	1
PVOUT3 Output Voltage 2	$V_{\rm VO32}$	PVOUT3=10mA	3.252	3.300	3.333	V	1
Line Regulation	V _{LINE}	PVOUT3=1mA AVIN=3.4 to 5.5V		0.05	0.25	%/V	1
Load Regulation	V _{LOAD}	1mA≦PVOUT3≦10mA		5	15	mV	1
Dropout Voltage	V _{IO}	PVOUT3=10mA AVIN=3.1V		0.10	0.18	V	1
Ripple Rejection 1 (Note5)	RR1	PVOUT3=1mA f=1kHz		60		dB	
Ripple Rejection 2 (Note5)	RR2	PVOUT3=1mA f=10kHz		40		dB	
Output Short-circuit Current (Note5)	I _{LIM}	VPVO3=0V		40		mA	
PVOUT3 Discharge Tr ON Resistance PVOUT3	R _{DVO3}	EN23=0V PVOUT3=3.3V		1		kΩ	2
Power Good							
P_GOOD1, 2 Detection Voltage	V _{PGAD}	Monitor AVIN Voltage AVIN=2.8→0V		V _{UVLOD} +50		mV	2
P_GOOD1 Detection Voltage	V _{PGFB1D}	Monitor FB1 Voltage FB1=0.6→0V	0.46	0.50	0.54	V	2
P_GOOD2 Detection Voltage	V _{PGFB2D}	Monitor FB2 Voltage FB2=0.6→0V	0.46	0.50	0.54	V	2
P_GOOD1, P_GOOD2 Release Voltage	V _{PGAR}	Monitor AVIN Voltage AVIN=0→2.8V	V _{PGAD} +100	V _{PGAD} +150	V _{PGAD} +200	mV	2
P_GOOD1 Release Voltage	V _{PGFB1R}	Monitor FB1 Voltage FB1=0→0.8V	V _{PGFB1D} +10	V _{PGFB1D} +25	V _{PGFB1D} +40	mV	2
P_GOOD2 Release Voltage	V _{PGFB2R}	Monitor FB2 Voltage FB2=0→0.8V	V _{PGFB2D} +10	V _{PGFB2D} +25	V _{PGFB2D} +40	mV	2
P_GOOD1, 2 "L" Output Voltage	V _{PGOL}	FB1=FB2=0V P_GOOD1, 2=10mA		0.12	0.30	V	2
P_GOOD1, 2 Pin Sink Current (Note5, 6)	I _{PGSINK}	FB1=FB2=0V P_GOOD1, 2=5V	100	150		mA	2
P_GOOD1, 2 Pin Leakage Current	I _{PGLK}	FB1=FB2=0.65V P_GOOD1, 2=6V	-1.0		+1.0	μΑ	2

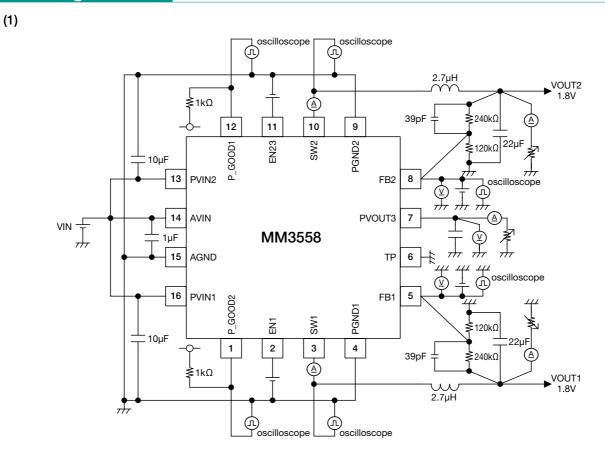
Note5 : The parameter is guaranteed by design.

Note6 : Please use it under Power dissipation. It shows in 13.TYPICAL APPLICATION CIRCUIT about calculation method of Loss.

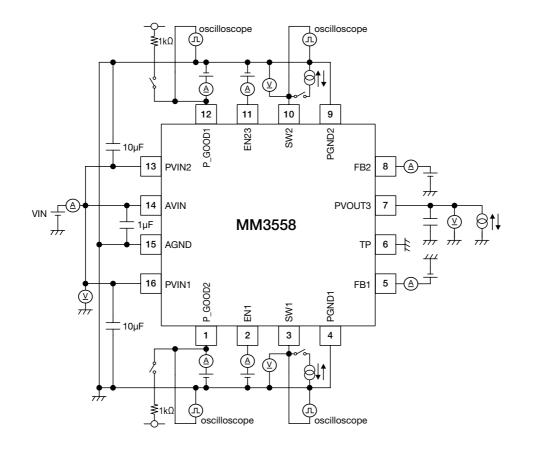
Item	Symbol	Measurement conditions	Min.	Тур.	Max.	Units	Measuring Circuit No.
Delay time							
Start / Stop Delay Time (Note7)	t _{stdly}	EN1, 23=0V⇔3V EN1 : Ch1 enable EN23 : Ch2, LDO enable		10		us	2
P_GOOD Detection Blanking Time During SoftStart (Note7)	t _{DTDLY_SS}			5.5× t _{ss}	8.3× t _{ss}	ms	1
P_GOOD Detection Blanking Time (Note7)	t _{DTDLY}	AVIN=4.5V \rightarrow V _{PGAD} , FB1(FB2)=0.6 \rightarrow V _{PGFB}		10		us	2
SW1, 2 Current Limit Timer Latch Time (Note7)	t _{LIMSWDLY}			1.5		ms	1

Note7 : The parameter is guaranteed by design.

Measuring Circuit



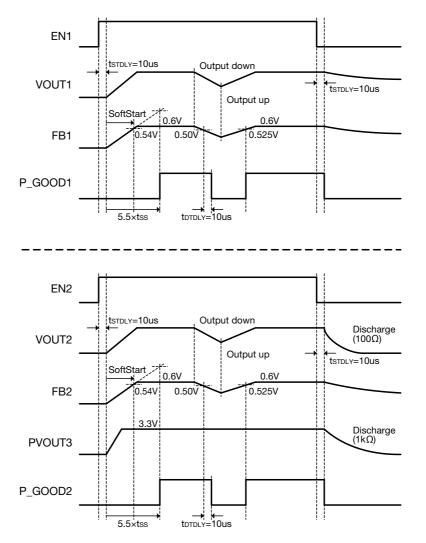
(2)



Timing Chart

(1) Each output start, stop timing

AVIN=PVIN1=PVIN2=5.0V



The delay time (10us typ.) has been set for the input of enable terminal EN1 and EN23. Therefore, IC-output doesn't response when a short signal of the cycle is input to an enable terminal at delay time.

(2) Protected operation

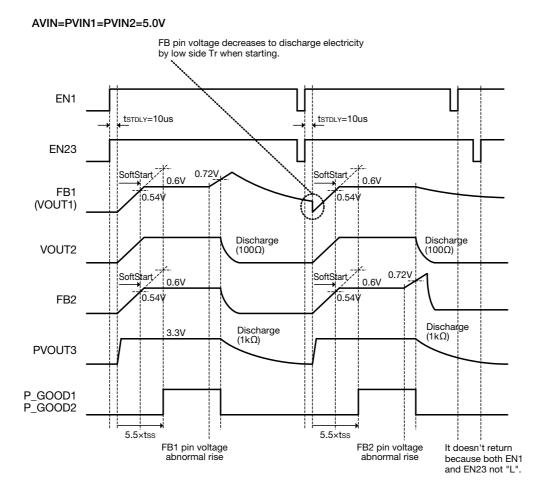
• UVLO detection, OVP_IN detection

AVIN=PVIN1=PVIN2=EN1=EN23 FB pin voltage decreases to discharge electricity by low side Tr when starting. 5.8\ 5.0V 5.0V 5.65Ū AVIN 2 7\ **PVIN** SoftStart 0.6V 0.6V FB1 0.54V . 54V (VOUT1) SoftStart SoftStart 0.6V 0.6V FB2 Discharge 0.54V 0.54V (100Ω) (VOUT2) 3.3V Discharge 3.3V (1kΩ) PVOUT3 P_GOOD1 P GOOD2 5.5×tss 5.5×tss AVIN 2.60V PVIN ⊒⊔≔ t<totute=10us) 2.55V 0.6V FB1 (VOUT1) 0.6V Discharge FB2 (VOUT2) (100Ω) Discharge PVOUT3 (1kΩ) P_GOOD1 P_GOOD2 tDTDLY=10us

When AVIN rises and the input overvoltage is detected, VOUT1, 2, and PVOUT3 are turned off. Operation can be returned by decreasing AVIN.

The P_GOOD changes to "L" in the condition of the AVIN \leq P_GOOD detecting voltage (Monitor AVIN voltage) after delay time. However, it doesn't respond for a signal of the cycle short following delay time.

• OVP_OUT detection

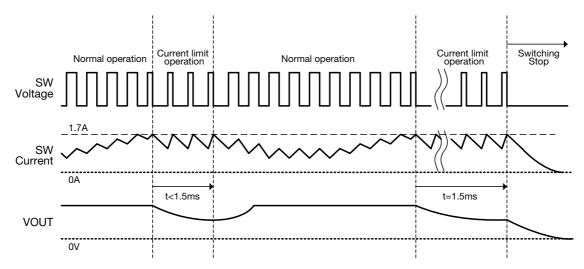


The output overvoltage protection circuit works when the DC/DC converter voltage of the FB pin exceeds 0.72V(TYP), the switching of SW1 and SW2 stops, the PVOUT3 output is turned off, and the state is maintained.

It is necessary to decrease AVIN below VIN UVLO detection voltage so that the FB pin may release (FB1, FB2< 0.72V) when released and the state of the latch from the state of the output overvoltage or to make both EN1 and EN23 "L".

(3) Over current protection

• Over current protection for DC/DC converter



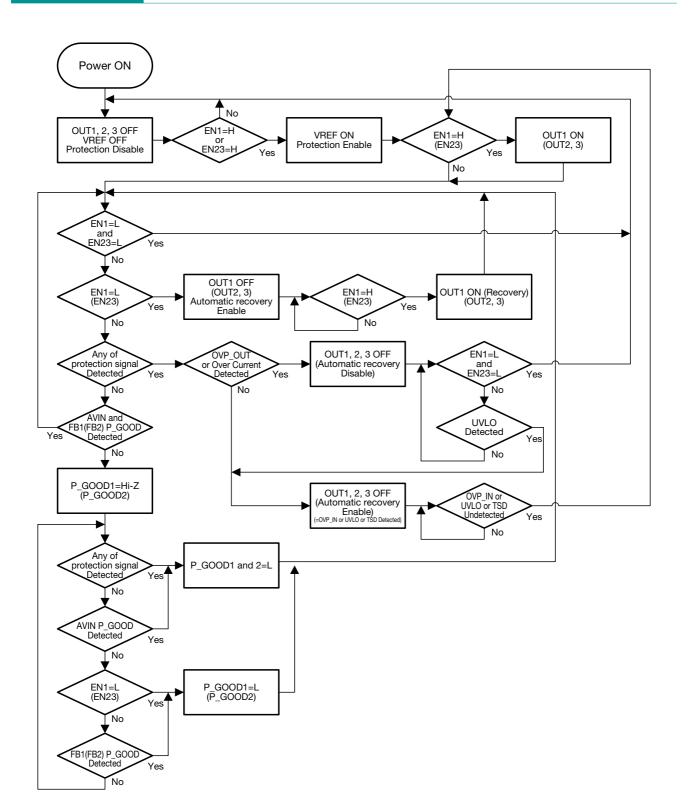
When a current limit is continuously detected between 1.5ms, the DC/DC converter maintains OFF state with the short-circuit protection circuit. And, both SW1 and SW2 switching are stopped, and the PVOUT3 output is turned off, too.

The output of the DC/DC converter and PVOUT3 returns by turning on both the re-turning on or EN1 and EN23 power supplies again.

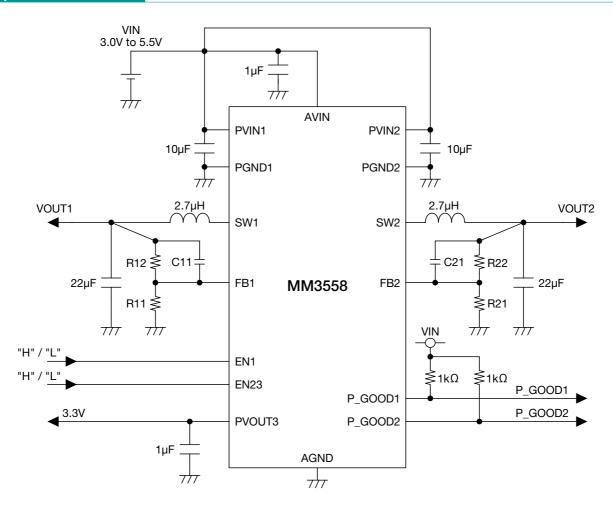
Over current protection for PVOUT3

Even if over-current protection of PVOUT3 is effective, it does not have the influence on DC/DC converter operation. The output of PVOUT3 will also return, if over-current protection of PVOUT3 is canceled.

Flow Chart



Application Circuit



Application notes

- (1) Setting of output voltage
 - $\cdot\,$ The output voltage can be calculated by the following expressions. VOUT1=0.6×(1+R12/R11)
 - $\cdot\,$ Please set not to exceed R11+R12=1M Ω from the reason for stability.
 - Please adjust for Zero points fz of the feedback loop to become 20kHz the value of C11 for the phase compensation. Zero points fz are calculated by the following expression. $fz=1/(2 \times \pi \times C11 \times R12)$
 - It becomes the best by adjusting fz according to the value of the usage, inductance, and the output capacity.
 - · Please set VOUT2 as well as VOUT1.
- (2) When PVOUT3 is not used
 - The capacitor of 1uF is recommended to be connected with the terminal even when PVOUT3 is not used.
 - There is a possibility of connecting it with the problem of an increase of the supply current etc. when the terminal is opened or it is used while it is short-circuited in the power supply.

- (3) About the calculation of IC loss
 - The substrate size mounts on two glass epoxy layer substrate
 (90% of rate of copper interconnect) to which it is referring in Note3 of the RECOMMENDED
 OPERATING CONDITIONS is computed for an example.
 - The power dissipation at 25°C to 150°C is computable with about 2.01 W from thermal resistance 62.2°C/W. For example, when carrying out the pull-up of the P_GOOD terminal to an external power supply, if it connects with 5V power supply directly, 150 mA (typ.) sink current will flow. As a loss of a P_GOOD terminal, PP_GOOD = 5V x 150mA = 0.75W occur.
 When P_GOOD1 and 2 both sides are set as the same conditions, since 1.5W (typ.) loss occurs, it is the calculation which generates heat about 93.3°C.
 By element variation, temperature variation, other losses in a circuit, and thermal resistance by substrate conditions, since a loss/calorific value is changed, please set up the conditions of a P_GOOD terminal after fully examining a loss and calorific value by the set of use.
- (4) About the output operation of 1.0V or less

 If an input-and-output voltage difference is large and ON Duty falls, it becomes impossible to take operation in the PWM mode stable like following figure A.

The stability of input voltage of operation over 1.0V or less is shown in figure B.

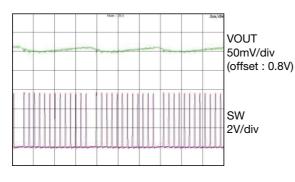


Figure.A Unstable operation waveform

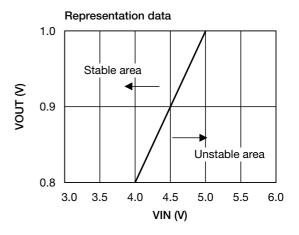
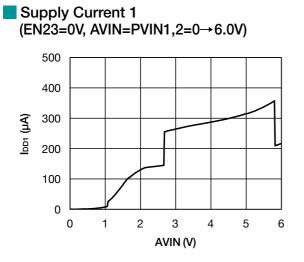
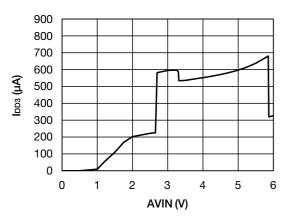


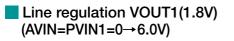
Figure.B 1V or less output vs VIN operation stability

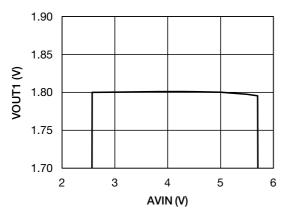
Characteristics (Except where noted otherwise Ta=25°C)

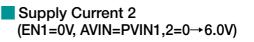


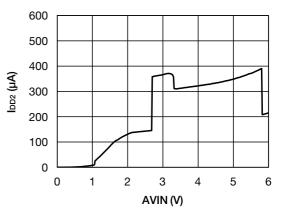
Supply Current (EN1=EN23=5V, AVIN=PVIN1,2=0→6.0V)



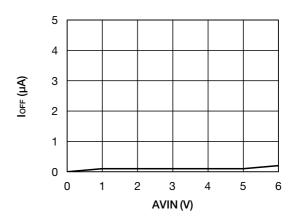


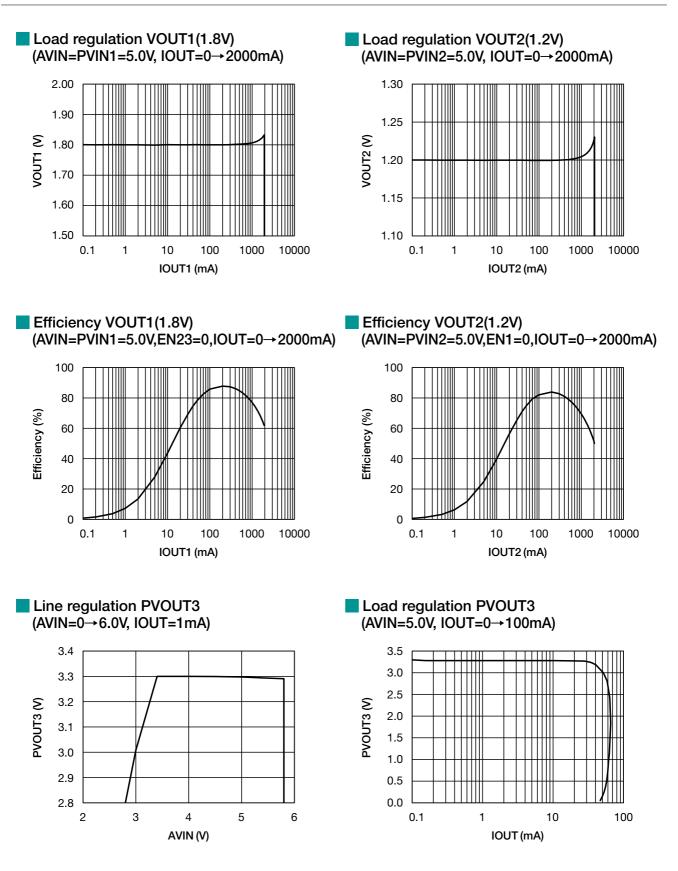




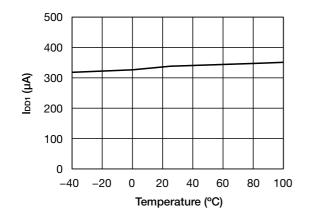


Shutdown Current (EN1=EN23=0V, AVIN=PVIN1,2=0→6.0V)

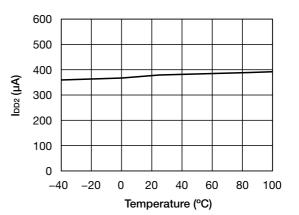


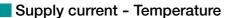


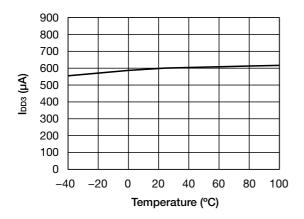
Supply current 1 - Temperature

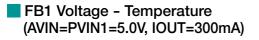


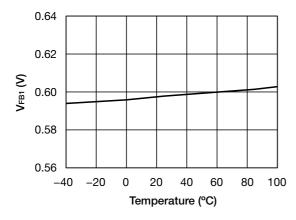
Supply current 2 - Temperature



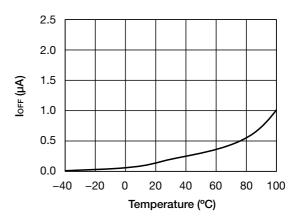




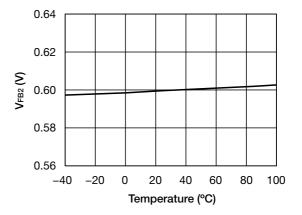




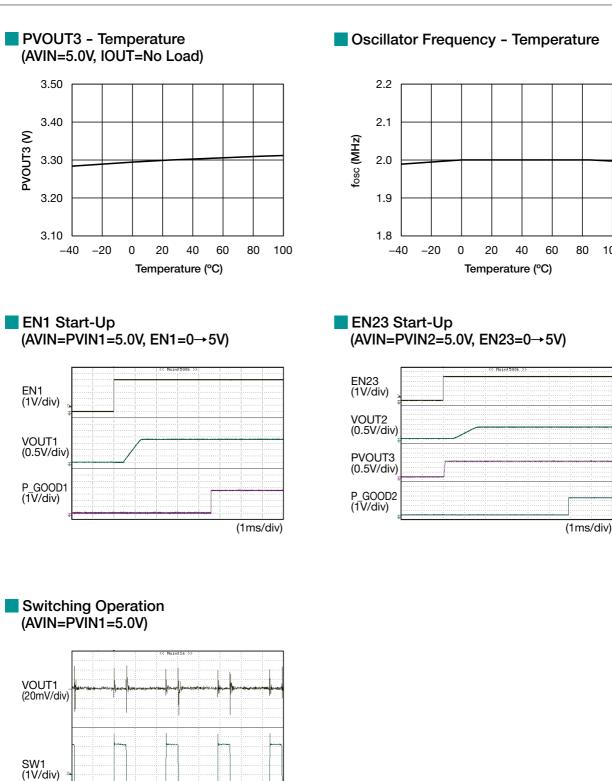
Shutdown current - Temperature



FB2 Voltage - Temperature (AVIN=PVIN1=5.0V, IOUT=300mA)



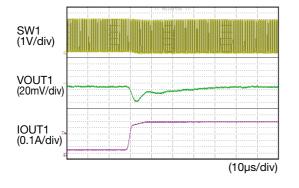
100



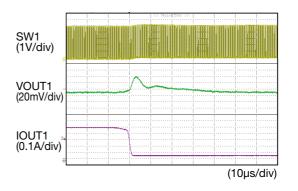
(200ns/div)

Load Transient Response

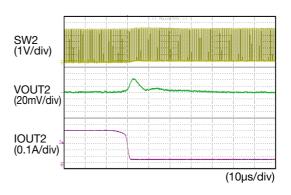
(AVIN=PVIN1=5.0V, VOUT1=1.8V, IOUT1=50mA→500mA)



(AVIN=PVIN1=5.0V, VOUT1=1.8V, IOUT1=500mA→50mA)



(AVIN=PVIN2=5.0V, VOUT2=1.2V, IOUT2=500mA→50mA)



(AVIN=PVIN2=5.0V, VOUT2=1.2V, IOUT2=50mA→500mA)

